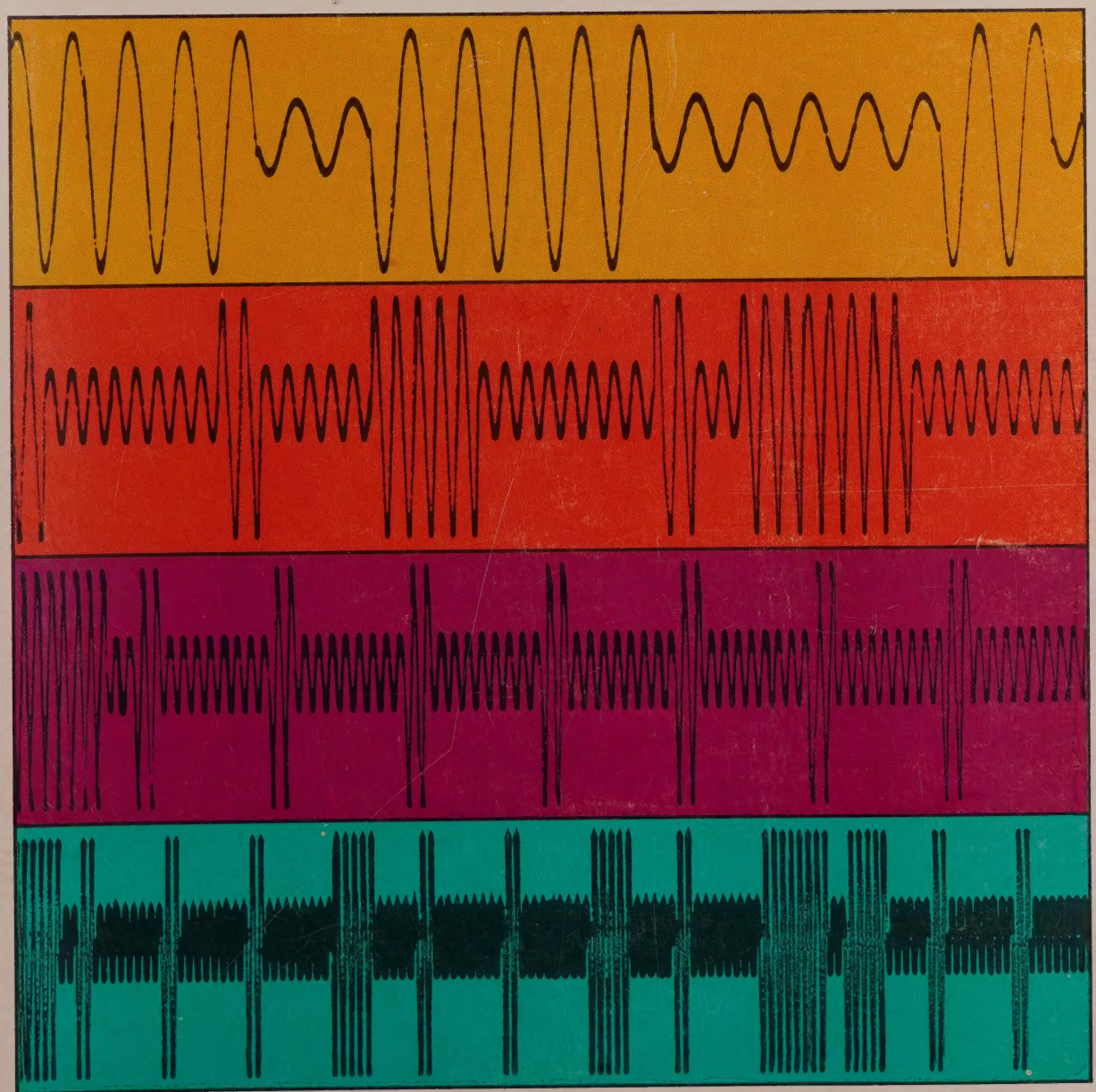
TIMING/SYSTEMS

INSTRUCTION MANUAL

SD 8520
Portable Time Code Generator



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SYSTRON-DONNER TIMING PRODUCTS
MODEL 8520
PORTABLE TIME CODE GENERATOR

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TABLE OF CONTENTS

			Page
CHAPTER 1	GENERAL DESCRIPTION		
	1.0	Basic Functions	1-1
	1.1	Portable Features	1-1
	1.2	Standard Features	1-2
	1.3	Applications	1-5
	1.4	Standard Optional Features	1-6
CHAPTER 2	INSTALLATION		
	2.0	Initial Inspection	2-1
	2.1	Storage and Reshipment	2-1
	2.2	Installation	2-2
	2.3	Power Requirements	2-2
CHAPTER 3	OPERATION		
	3.0	General	3-1
	3.1	Use of Controls, Indicators, and Connector	3-1
	3.1.0	Power Switch	3-1
	3.1.1	Battery Display Switch	3-2
	3.1.2	Mode Control	3-2
	3.1.3	Clock Adjust	3-4
	3.1.4	Time Display	3-5
	3.1.5	Mod Code J3	3-5
	3.1.6	Dc Code J4	3-5
	3.1.7	Pulse Rate Outputs J6 J7 J8	3-5
	3.1.8	Ext Sync J5	3-5
	3.2	Operation	3-6
	3.2.0	Turn On Procedure	3-6
	3.2.1	Reset Procedure	3-6
	3.2.2	Preset Time Procedure	3-6
	3.2.3	Stop Procedure	3-7
	3.2.4	Manual Start Procedure	3-8
	3.2.5	Automatic Start Procedure	3-8
	3.2.6	Synchronization Procedure	3-9
CHAPTER 4	MAINTENANCE AND CALIBRATION		
	4.1	Factory Service	4-1
	4.2	Routine Maintenance	4-1
	4.3	Printed-Circuit Board Repair	4-1
	4.4	Logic Functions	4-2
	4.5	JK-Type Flip-Flops	4-3
	4.6	Operational Test and Calibration Procedure	4-3
	4.6.1	Recommended Test Equipment	4-4
	4.6.2	Power Supply	4-4
	4.6.3	Switching Regulator	4-4
	4.6.4	AC Supply	4-4

TABLE OF CONTENTS
(continued)

			Page
CHAPTER 4	MAINTENANCE AND CALIBRATION		
	4.6.5	Time Base and Oscillator	4-4
	4.6.6	Adv/Ret Synchronizer	4-6
	4.6.7	Control, Input/Output	4-6
CHAPTER 5	OVERALL FUNCTIONAL DESCRIPTION		
	5.1	Time Base Adv/Ret Syncrhonizer	5-1
	5.2	Time Base, Minor Counters	5-1
	5.3	BCD/10 Line Dual Decoder	5-1
	5.4	Control, Input/Output	5-1
	5.5	Accumulator Cards, Seconds, Minutes, Hours	5-1
CHAPTER 6	CIRCUIT DESCRIPTIONS		
	6.1	Time Base/Adv-Ret Synchronizer	6-1
	6.2	Time Base/Minor Counters	6-7
	6.3	BCD 10 Line Dual Decoder	6-12
	6.4	Seconds Accumulator	6-19
	6.5	Minutes Accumulator	6-24
	6.6	Hours Accumulator	6-28
	6.7	Control, Input/Output	6-32
	6.8	Power Supply	6-39

LIST OF DIAGRAMS

Title	Dwg. #	Page
Schematic Time Base/Adv-Ret Synchronizer	62211-7202 G2	6-6
Time Base/Minor Counters	62112-7502 G1	6-11
BCD - 10 Line Dual Decoder	62211-7201 G1	6-14
Optional Codes & Code Formats		6-15 thru 6-18
Seconds Accumulator	62112-7504 G1	6-23
Minutes Accumulator G1	62112-7505 G1	6-27
Hours Accumulator G2 and G4	62112-7505 G2 & G4	6-31
Control Input/Output	62112-7508 G2	6-37
Timing Diagram DC Code G3		6-38
Power Supply	62211-7306 B	6-49
AC Power Supply	62211-7114	6-50
Switching Regulator	62211-7307	6-51
Heater Circuit	62211-7305	6-52
Readout, Front Panel	62211-7203 G2	6-53
8520 & 8521 System Block Diagram	62211-0001	6-54
Main Chassis Wiring Diagram	62211-7001 C	6-55

MODEL 8520

CHAPTER 1

GENERAL DESCRIPTION

1.0 BASIC FUNCTIONS

The Model 8520 is an extremely rugged, integrated circuit logic (discrete components used where required) Portable Time Code Generator (PTCG) which generates the standard serial time code Inter Range Instrumentation Group "B" (IRIG B) or XR 3 (optional) Binary Coded Decimal (BCD) Format and displays them in terms of hours, minutes, and seconds and provides outputs to drive other displays.

IRIG B or XR-3 (optional) Time Codes are provided as both a modulated format and a dc level shift output. Pulse outputs of 1000 p/s, 100 p/s, and 1 p/s are available at BNC connectors on the unit front panel. Time-of-day information may also be provided as parallel BCD outputs for remote displays and/or remote controls and display units (option E15).

An External pulse input allows for synchronization to an external source such as WWV, and Advance/Retard circuitry allows for retaining synchronization after initial start coincidence.

1.1 PORTABLE FEATURES

Some portable features are cited in Table 1.1.

TABLE 1.1

PORTABLE FEATURES

Self-contained Numeric Display (Hrs., Min., Sec.)

TABLE 1.1
(continued)

Light Weight:	15 pounds
Small Size:	4-7/8" wide 7-5/8" high 12-1/2" deep handles add approximately 1-1/2" to height.

All operating Controls for Start/Stop, Preset, Reset, Advance/Retard, Battery Display, etc.

(Self-contained 45 minute rechargeable Battery Pack.)

1.2 STANDARD FEATURES

The Model 8520 PTCG is designed for simple reliable operation, long life, and easy maintenance. Its circuitry is fully solid-state and constructed on printed circuit plug-in modules. It has a six-digit in-line readout which displays time-of-day information continuously in terms of hours, minutes, and seconds.

A brief summary of the Model 8520 PTCG standard features is cited in Table 1.2 and are elaborated on in other areas of this manual.

TABLE 1.2

MODEL 8520 PORTABLE TIME CODE GENERATOR

SERIAL TIME CODE:

IRIG "B" or XR 3 (optional) Format in terms of BCD hours, minutes, and seconds.

MODULATED CODE:

Carrier Frequency: IRIG "B" - 1 kHz; XR 3 1 kHz or 250 Hz.

Level - Adjustable from 0 to 10 volts peak-to-peak from a low impedance 15 mA current source.

TABLE 1.2
(continued)

Modulation Ratio: 3:1 nominal, adjustable from 2:1 to 6:1.

Connector - Front panel BNC.

DC LEVEL SHIFT:

0 ±0.4 V dc to +5 V dc peak from a 5 mA source.

CONNECTOR:

Front panel BNC

DISPLAY:

Six (6) miniature in-line display tubes display time of day in terms of hours, minutes, and seconds.

TIME BASE:

1 MHz crystal controlled oscillator

STABILITY:

Aging rate 1 part 10^7 per day. 1 part 10^5 -20°C to +55°C.

PULSE OUTPUTS:

1000 p/s. 100 p/s, 1 p/s leading edge "on time".

LEVEL: 0 ±0.4V dc to a +5 V dc peak from a 5 mA source. Rise time 0.5 microseconds.

CONNECTOR:

Front Panel BNC

SYNCHRONIZATION:

From an external 1 p/s such as WWV tick envelope.

BATTERY PACK:

A self-contained 45 Minute rechargeable nickel cadmium unit (-20°C to +65°C.)

POWER:

12 to 50 V dc; 0.7 amp at 28 V dc. 117/230 V ac ±10% 50-400 Hz OPTIONAL.

PACKAGING:

4-7/8" x 7-5/8" x 12-1/2 deep. Feet and handle add approximately 1-1/2" to height.

MANUAL CONTROLS:

Power - ON/OFF Switch, Locking toggle, Power Fuse, and Indicator.

Mode Control -

*START RUN MIN HR STOP Rotary Switch

*PRESET (HR or MIN) FAST 5/second, Slow 1/second, momentary toggle switch

*RESET HR MIN Momentary toggle switch

Clock Adjust -

*ADVANCE/RETARD momentary switch

*PER SEC Rotary rate selector of 100 ms, 10 ms, 1 ms, 100 µs and OFF.

TABLE 1.2
(continued)

Battery Display - Momentary Toggle Switch

ENVIRONMENTAL

Shock/ Vibration - Mil E5400 Class II

Humidity - 95%

Operating Temperature - -20°C to +65°C

Storage Temperature - -55°C to +100°C

RFI

Mil 6181D

1.3 APPLICATIONS

The 8520 PTCG allows maximum flexibility in configuration choice based upon actual job requirements in the following fields of test data recording:

1. Aircraft (fighter, bomber, transport, commercial)
2. Automotive
3. Trains
4. Helicopters
5 Medical
6. Geophysics (Earth Motion Studies)
7. Shipboard
8. Life Test Analysis

1.4 STANDARD OPTIONAL FEATURES

The Design of the Model 8520 PTCG, while allowing the user to meet his particular configuration requirements, is essentially that of the 8521 Airborne Time Code Generator (ATCG).

With Specific Standard Options (Table 1.3) Available for the 8520 PTCG the user could match his needs and attain an Airborne Configuration. These options include:

1. Shock Mounts
2. Wide Temperature Operation
3. Remote Control
4. High Stability Oscillator

TABLE 1.3

8500 SERIES STANDARD OPTIONS

MODEL	OPTION	DESCRIPTION
8520		Portable Time Code Generator. Provides IRIG B (BCD) modulated and dc code outputs plus pulse rates. Synchronizable; advance/retard control. Operates from 12 to 50 volts dc; has built-in Nicad battery pack for backup. Weighs 15 lbs.
	B14	High Stability Oscillator. 5×10^{-7}/day from -40 to +65°C with zero warmup time.
	E15	Add Connector for remote control and display unit or remote display unit.
	L12	Ac Power Pack. Provides ac operation (in addition to dc) of 117/230 volts, 48 to 440 Hz. (add 4 lbs).
	M11	Extended Temperature operation (-55 to +65°C).
	M13	Add Shock Mount adaptor (includes all-angle shock mount).
	C26A	Substitute XR 3 Code on 1 kHz carrier for IRIG B.

TABLE 1.3
(continued)

MODEL	OPTION	DESCRIPTION
8520		
	C26B	Substitute XR 3 Code on 250 Hz carrier for IRIG B.
8521		Airborne Time Code Generator. Same as 8520 but requires remote control and display unit. Includes high stability oscillator, extended temperature operation and shock mount. Weighs 15 pounds.
	L12	Ac Power Pack. Provides ac operation (in addition to dc) of 117/230 volts, 48 to 440 Hz (add 3 lbs.)
	M12	Portable Kit. Remove shock mount adaptor and add carrying handle and feet.
8580		Remote Display Unit. Hours, minutes, and seconds.
8585		Remote Control and Display Unit

NOTES: 8500 Series

1) To use Model 8580 or Model 8585 with Model 8520 Portable, Option E15 must be added to Model 8520.

CHAPTER 2

INSTALLATION

2.0 INITIAL INSPECTION

As soon as the Model 8520 PTCG is received, verify that the instrument is intact, and as ordered. To insure that all Printed Circuit boards (PC boards) are firmly seated in their proper mating connector as indicated by the silkscreen on the side of chassis, (refer to Figure 2-1), the PTCG may be removed from its cover by means of loosening the 1/4-turn DZUS screw fastener at the back of the unit. If shipping damage is found, refer to the warranty (inside of this manual's back cover) and Paragraph 2.1 for repackaging instructions.

2.1 STORAGE AND RESHIPMENT

Environmental conditions during storage and reshipment should be limited as follows:

a. Maximum temperature +100°C

b. Minimum temperature -55°C

To protect your instrument during shipment or storage, use the best packaging methods available. Your SYSTRON-DONNER field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable custom packaging on short notice.

If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb. sq. inch bursting strength) or wooden box to house the instrument.

a. Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

b. Use plenty of packing material around all sides of the instrument and protect front panel with cardboard strips.

c. Seal the package with strong tape or metal bands. Mark with "DELICATE INSTRUMENT".

d. Refer to Warranty Page (inside rear cover of this manual) and check with SYSTRON-DONNER field office for shipping instructions. All correspondence should refer to an instrument by model number and the full serial number.

2.2 INSTALLATION

All Model 8520 PTCG's are shipped in a fully operable condition and require no special installation instruction except when ordered with certain optional features, (in which case) addendum sheets cover the special installation instructions.

Simply connect power cable and refer to CHAPTER 3 for Operating Instructions.

2.3 POWER REQUIREMENTS

The Model 8520 PTCG is designed for operation from a power source 12 to 50 V dc. The internal Battery Pack should be disconnected for inputs below 22 V dc as this will discharge the pack.

AC POWER PACK OPTION

Provides ac operation (in addition to dc operation) of 117/230 volts, 50 to 400 Hz. A simple internal switch change is performed for either 117 or 230 volt operation. This option adds approximately 4 pounds to the overall weight. Operation on ac or on dc inputs above 24 volts will maintain the internal battery pack in a fully charge condition.

CHAPTER 3

OPERATION

3.0 GENERAL

The Model 8520 PTCG is ready to operate immediately after turning on the power switch. The 1 MHz crystal controlled oscillator has an aging rate of 1 part of 10^7 per day with a stability which exceeds 1 part 10^5 per day over the operational temperature range of -20°C to +55°C. No warmup time is required within this range to achieve this stability. No preliminary adjustments or calibration procedure is necessary. It is advisable to read the following descriptions before using the PTCG.

3.1 USE OF CONTROLS, INDICATORS, AND CONNECTORS

The following paragraphs and photograph in Figure 3.1 illustrates the operation, location, and use of the Model 8520 PTCG's controls, indicators, and connectors.

3.1.0 Power Switch

The Power (up is ON, down is OFF) switch S1 is a locking toggle switch, which when placed in the ON position locks itself ON and the ON light is lighted. When placed in the OFF position it locks itself OFF and the ON light is deenergized.

If the MODE CONTROL switch is in the START or RUN position when the Power switch is placed in the ON position, the PTCG will display an arbitrary time-of-day and begin counting. If in other positions of the MODE CONTROL switch when the Power

switch is placed in the ON position, numerals will be illuminated and possibly double numerals will appear but no count will occur when the Power Switch is placed in the ON position. The PTCG should be RESET, then PRESET to a desired count before proceeding.

3.1.1 Battery Display Switch

During battery operation of the PTCG (battery operation is started automatically without time loss in case external power fails), the numerical indicators are not illuminated to conserve battery life. To read the numerical indication during battery operation, hold the BATTERY DISPLAY switch S7 (a momentary switch) in the up position.

3.1.2 Mode Control

Mode Control utilizes 3 separate switches to perform the Mode Control Function and allow start time accuracy to approximately 1 second. The three Mode Control switches are cited and described below:

a. PRESET S3 (FAST or SLOW) (MIN or HR) momentary toggle switch, center off.

b. RESET S4 MIN HR momentary toggle

c. START RUN MIN HR STOP S2 rotary

3.1.2.0 PRESET S3 (FAST or SLOW) will set either minutes or hours to a predetermined start time if S7 is in MIN or HR position and the unit previously started. FAST rate is 5 hours or minutes per second. SLOW rate is 1 hours or minute per second.

3.1.2.1 RESET S4 will reset the seconds, minutes, and hours accumulator to zero if S7 is in MIN or HR position independent of the previous operating MODE of the unit.

3.1.2.2 START RUN MIN HR STOP switch S7 functions as follows:

a) START position forces manual starting of the minor counter chain and updating of the time-of-day accumulator. It permits subsequent presetting of the unit after initial application of power or after MODE switch has been in the STOP position.

b) RUN position allows external automatic starting of the minor counter by means of a momentary closure to ground derived from some external source such as the WWV 1 second tick signal.

c) MIN or HR position allows for resetting of the entire time accumulator (seconds, minutes, hours) or presetting of time in minutes or hours into the accumulator for some later start time.

The time of day accumulator is disconnected from the minor counter in the MIN or HR position causing the seconds display to remain stationary, however, the PRESETTING function requires that the minor counter chain be running to obtain the rates necessary for updating the MIN or HR accumulator with the PRESET switch. This can be accomplished in two ways. If real time is of no great importance or a time reference signal is not available, the MODE switch should

be placed in the START position then moved to the HR, MIN position. If a time reference signal is available, it is connected to the EXT SYNC (J5) input. The MODE switch is placed in the STOP position then moved to the HR position. The next occurrence of the reference signal will start the minor counter and allow presetting.

d. Stop position enables the control circuitry to stop the minor counter at the exact occurrence of the PTCG's 1 p/s. When the optional REMOTE CONTROL unit is used in conjunction with the PTCG the calculated propagation delay of a received reference signal, such as WWV, can be added to the 1 p/s STOP signal so that subsequent starting of the minor counter with that reference signal will compensate for the signal delay, and start the minor counter within 100 μs of the external reference signal.

3.1.3 Clock Adjust

Clock Adjust utilizes 2 separate switches to perform precise real time alignment of the PTCG 1 p/s in synchronization with some outside 1 p/s source such as WWV.

ADV RET switch S6, a momentary toggle used in conjunction with the PER SEC rotary switch S5, permits time to be added or subtracted at four decade rates from 100 microsecond per second, to 100 millisecond per second.

3.1.4 Time Display

Time is displayed in hours, minutes, and seconds by means of a horizontal array of six ultra-long-life cold cathode numerical display tubes, mounted behind a polarized filter for reduction of glare. Normal maximum viewing distance for the 0.5 inch high neon red characters is 24 feet.

3.1.5 Mod Code J3

The MOD CODE BNC connector (J3) is the output connector for the modulated serial Binary Coded Decimal (BCD) code representing time in hours, minutes, and seconds with a carrier frequency of (1 kHz IRIG B) or (1 kHz or 250 Hz XR 3). The MARK output level is adjustable from 0 to 10 V peak-to-peak from a low impedance 15 mA current source. The Modulation ratio MARK to SPACE is adjustable from 2:1 to 6:1 nominally set to 3:1.

3.1.6 Dc Code J4

The Output Level Shift Code J4 (dc CODE) dc level for IRIG B or XR 3 BCD code is 0 (±0.4) volts to +5 volts clamped into a 1 kΩ load. Positive going edge is (on time).

3.1.7 Pulse Rate Outputs J6 J7 J8

Three simultaneous pulse trains are provided at rates of 1 k p/s J6, 100 p/s J7, and 1 p/s J8 at their individual BNC connectors. Output level for each is 0 ±0.4 V dc to +5 V dc peak from a 5 mA current source. Rise time is approximately 0.5 microseconds.

3.1.8 Ext Sync J5

The EXT SYNC BNC J5 connector is the input from some external

1 p/s time reference signal such as WWV tick envelope for synchronization of the PTCG (see 3.1.3 and 3.2.5).

3.2 OPERATION

A step by step operating procedure is outlined in the following paragraphs.

3.2.0 Turn On Procedure

a. Insure that dc power is supplied correctly to POWER INPUT connector J1; i.e., +28 V dc measured between pin C to A of J1's mating connector. Check that the fuse F1 is installed and of proper value: 2 amperes (2A 3AG).

b. Place power switch in the up (ON) position.

3.2.1 Reset Procedure

The 8520 cannot be reset with the MODE switch S2 in positions other than HR or MIN.

a. Place MODE switch S7 in HR or MIN.

b. Place the RESET switch S4 in the up position momentarily. The display will now indicate all zeros and all zeros are set into the seconds, minutes, and hours accumulator for a specific future start time.

3.2.2 Preset Time Procedure

a. Set S2 Rotary switch to START position, then to HR position.

b. Reset (see 3.2.1) to clear the arbitrary numerals appearing on the 6 digit time display.

c. Place S3 PRESET momentary toggle to FAST or SLOW and set in desired time in hours.

d. Set S2 Rotary switch to the MIN position.

e. Place S3 PRESET momentary toggle to FAST or SLOW and set in the desired time in minutes. The time displayed is also the time set into the minutes and hours accumulators.

3.2.3 Stop Procedure

A STOP procedure is necessary in order that the TIME BASE/MINOR COUNTER register may be started "On Time" by being stopped in a known preset condition (see 3.1.2.2 d). STOP is effected merely by placing MODE CONTROL S2 in the STOP position.

The 8520 PTCG with NO Remote Control unit will stop with 000.00 milliseconds stored in the register, therefore, it will start "On Time" from an outside "On Time" electronic reference signal and provide an update signal to the time of day accumulator exactly one second later.

The 8520 PTCG operating with a Remote Control unit will stop with the time PRESET into the propagation delay switches of the Remote unit stored in the TIME BASE/MINOR COUNTER register. A SYNC signal with a known delay up to 99.9 milliseconds can then be used to start the PTCG "On Time".

3.2.4 Manual Start Procedure

a. Place the MODE switch (S7) to the START position at the moment the time equals the preset time. Time will now accumulate from this moment and the display will advance once each second.

b. After a manual start, the PTCG may be adjusted as outlined in Paragraph 3.2.6.

3.2.5 Automatic Start Procedure

The following procedure is used to synchronize the internal 1 p/s with an external WWV signal. Any WWV signal adjusted to an amplitude of approximately 5 V peak-to-peak may be used. The correct amplitude for signals having large noise content will have to be determined by experiment i.e., viewing the output of A7 Pin A/15 and externally adjusting the WWV input for a 1 p/s pulse output of the required amplitude.

a. Connect the external 1 p/s reference to EXT SYNC connector (J5).

b. Set the MODE CONTROL switch (S2) to the RUN position.

c. The internal 1 p/s reference of the 8520 PTCG is now synchronized with external 1 p/s reference and updated time is being displayed. The external reference may now be removed.

NOTE: Although the internal reference is now "on time", the clock has not been set to the correct time-of-day. This may be accomplished by the procedure outlined in Paragraph 3.2.6. As long as the MODE CONTROL switch (S2) is not placed in STOP

position, this procedure will not cause loss of internal reference synchronism, since, although the readout is stopped, the internal 1 p/s reference is still being generated and maintains the sync which has been established.

3.2.6 Synchronization Procedure

In order to precisely sychronize the 8520 PTCG, the following test equipment is required. Oscilloscope Tektronix Model 535 or equal, Precision Time Source WWV, Laboratory Clock, etc. Once the 8520 PTCG has been started, it may be desirable to synchronize, particularly, if the Manual Start procedure has been used. The following procedure may be used and will not require resetting the clock.

1. Connect a time standard such as WWV to one vertical axis input of a dual trace oscilloscope.

2. Connect the 1 p/s output from the 8520 PTCG connector (J8) to the second vertical axis input of the scope.

3. Ascertain that the PTCG is displaying time within 1 second of the correct time as received from the reference signal. This may be done by a visual check of the laboratory clock or by monitoring the audio WWV announcement.

4. Superimpose the two traces on the oscilloscope and determine whether the internal 1 p/s signal is leading or lagging the external 1 p/s reference.

5. Set the CLOCK ADJUST PER SEC switch (S5) to a rate that will

correct for the difference between the two pulses in a few seconds.

6. In the internal 1 p/s is lagging, place the ADV/RET switch (S6) in ADV position and hold until the leading edge of both pulses are perfectly coincident. If the internal 1 p/s pulse is leading, use, the RET position of S6. In either case, the switch will return to the neutral position when released.

7. For a more exact synchronization, expand the time base on the oscilloscope and repeat the above procedure using a slower Rate/Second setting of S5.

CHAPTER 4

MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

Whenever the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns when necessary. Address all inquiries on operation or applications to your nearest sales representatives, or to:

Sales Manager, SYSTRON-DONNER CORP.
1 Systron Drive
Concord, California 94520

Specify both model and complete serial number in all correspondences.

4.2 ROUTINE MAINTENANCE

A regular program for routine maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

(1) Disconnect power and remove the cover.

(2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.

(3) Check for physcial integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed circuit board contains integrated circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

(4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

(5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove the foreign material.

CAUTION

Do not clean PC boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device not be used on small internal components.

(6) Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints, and other foreign material.

(7) Replace the cover and reconnect power. Perform the Operational Test and Calibration Procedure (Paragraph 4.6). If performance does not match or exceed the specifications listed in Chapter I of this manual, corrective maintenance is in order.

4.3 PRINTED-CIRCUIT BOARD REPAIR

To remove a part on a printed-circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts of less) soldering iron, apply heat sparingly to each cut lead. As soon as the solder melts, slip the lead from the hole and clean the hole with a toothpick. Clean the board surfaces with isopropyl alcohol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16 inch beyond the back surface of the board. Only 63/37 solder with a maximum diameter of 1/16 inch should be used. Solder the leads to the board and use a hemostat, long-nosed pliers, or other

heat sink on the leads of all semiconductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

4.4 LOGIC FUNCTIONS

The logic symbols and functions, as used in the Model 8520/8521, are described in the following paragraph. Truth tables and detailed explanations are given where necessary in order to assist qualified maintenance personnel in the repair and upkeep of the instrument.

AND Gate

OR Gate

NAND Gate

INVERTED OR Gate

The NAND Gate and the INVERTED OR Gate have the same truth tables.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

INVERTED AND Gate

The NOR Gate and the INVERTED OR Gate have the same truth tables.

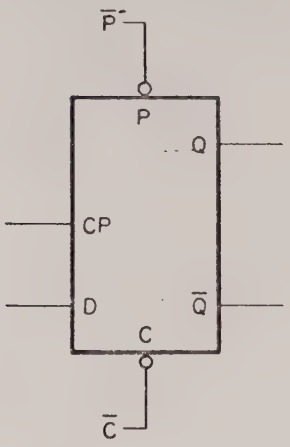
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

DOT AND

DOT OR

In some configurations it is possible to perform the AND and OR function simply by tying the outputs of certain gates together. These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line, the AND or OR symbol is used only once.

D-TYPE Flip-Flop



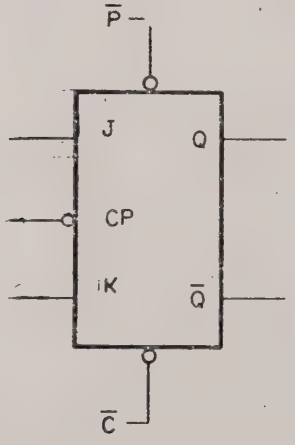
(1) Q assumes the start of the D input on the positive transition of the clock (CP) input.

(2) The D input is locked out when the clock input is positive.

(3) $\overline{P}$ and $\overline{C}$ override all other inputs.

(4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.

(5) At a preset condition, Q is a Logic 1. At clear condition, Q is a Logic 0.



J = J1•J2•J3

K = K1•K2•K3

4.5 JK-Type Flip-Flop

(1) If J and K are both at Logic 0 when the clock input ($\overline{CP}$) assumes a Logic 0 state there is no change in the output.

(2) If K is a Logic 1, Q will assume a Logic 0 when $\overline{CP}$ goes to Logic 0.

(3) If J is a Logic 1, Q will assume a Logic 1 when $\overline{CP}$ goes to Logic 0.

(4) If J and K are both at Logic 1 the flip-flop will change state when the clock input is Logic 0.

(5) The J and K inputs are locked out when the clock input is Logic 0.

(6) $\overline{P}$ and $\overline{C}$ override all other inputs.

(7) If $\overline{P}$ and $\overline{C}$ are both at Logic 0 the Q and $\overline{Q}$ outputs are both at Logic 1.

(8) At the preset condition, Q is a Logic 1.

4.6 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the technician to isolate the trouble to a particular circuit card.

When the trouble is isolated to a card, the card description in Chapter 6 will facilitate repair.

WARNING

DANGEROUS HIGH VOLTAGES ARE PRESENT IN THE POWER SUPPLY AND DISPLAY CIRCUITS OF THIS EQUIPMENT. USE CAUTION AT ALL TIMES WHEN THE PROTECTIVE COVERS ARE REMOVED.

4.6.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8520/8521.

MODEL	MANUFACTURER	DESCRIPTION
535A	TEKTRONIX, INC.	Oscilloscope, 15 MHz Bandwidth triggered sweeps from 0.1 microseconds/cm to 5 sec/cm.
CA	TEKTRONIX, INC.	Dual-Trace Calibrated preamp for 535A scope, 0.05 volts/ cm to 20 volts/cm.
P6000	TEKTRONIX, INC.	Probe, 10:1 Attenuation Ratio, 12 pf of capacitance.
9000	SYSTRON-DONNER CORPORATION	VOM, 10 MΩ input impedance, ±0.1% accuracy.

In addition to the equipment listed above, a receiver capable of receiving WWV is required to accurately check the WWV sync circuit. To test the ADVANCE/RETARD system (especially the slower rates), another time code generator should serve as a 1 pps reference. Lacking another TCG, any reliable 1 pps source may be used.

4.6.2 POWER SUPPLY Dwg. 62211-7306 and 62211-7307

The voltage checks listed below will insure the correct operation of the power supply assuming that the 12 V adjust is properly set (refer to paragraph 4.6.3).

(1) Insure the presence of +200 V dc ±20% on Pin B/16 of A8.

(2) Insure the presence of +5 V dc ±0.5 V on the +5 V buss, (on the underside of the chassis with many red wires on it).

4.6.3 SWITCHING REGULATOR Dwg. 62211-7306 and 62211-7307

The switching regulator maintains 12 V dc for the DC to DC converter. The voltage is adjusted by monitoring the 5 V buss and setting R14 to give +5 V dc ±0.5 V. This is the only adjustment in the power supply.

4.6.4 AC SUPPLY Dwg. B62211-7114

This plug-in unit has provision for using either 115 or 230 V ac input. Be certain that the selector switch is set correctly for the line voltage being used.

4.6.5 TIME BASE AND OSCILLATOR Dwg. 6211-7202

The accuracy of the oscillator may be determined, relative to a frequency standard, by observing the rate of drift of an oscilloscope pattern as shown in Figure 4.1, the oscillator accuracy test diagram.

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard;

if the pattern moves to the left, the freuqency under test is too high.

To check oscillator frequency (not stability):

(1) Trigger the oscillscope externally with the 1 MHz internal oscillator of the 8520/8521.

(2) Connect a 1 MHz frequency from an external standard to the vertical input of the oscilloscope.

(3) Set the oscilloscope sweep time to 0.1 μsec/cm and adjust the controls to obtain a presentation of a 5 V peak-to-peak waveform.

(4) Horizontal drift of the oscilloscope display in cm/sec is the difference from the standard frequency in parts/10 . If necessary adjust the oscillator.

(5) To adjust the standard oscillator vary the setting of C9 on the TIME BASE, ADV/RET SYNCHRONIZER card. To adjust the high stability oscillator, remove the screw covering the adjustment capacitor and vary the setting.

(6) Verify the presence of a 100 k pps signal at Pin B/18 and 500 k pps at Pin B/17.

TABLE 4.1
OSCILLATOR ACCURACY

Drift	Accuracy
1 cm/0.1 sec	1 part in 10 (10 Hz)
1 cm/sec	1 part in 10 (1.0 Hz)
1 cm/10 sec	1 part in 10 (0.1 Hz)

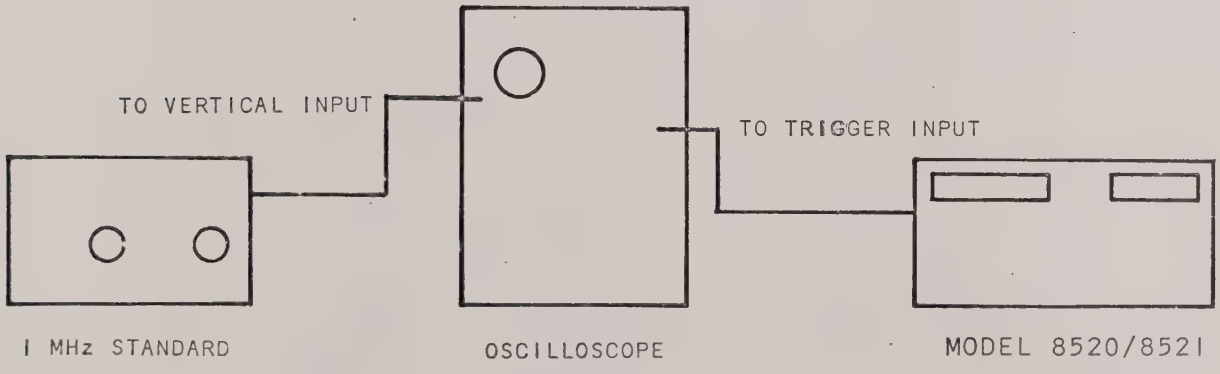
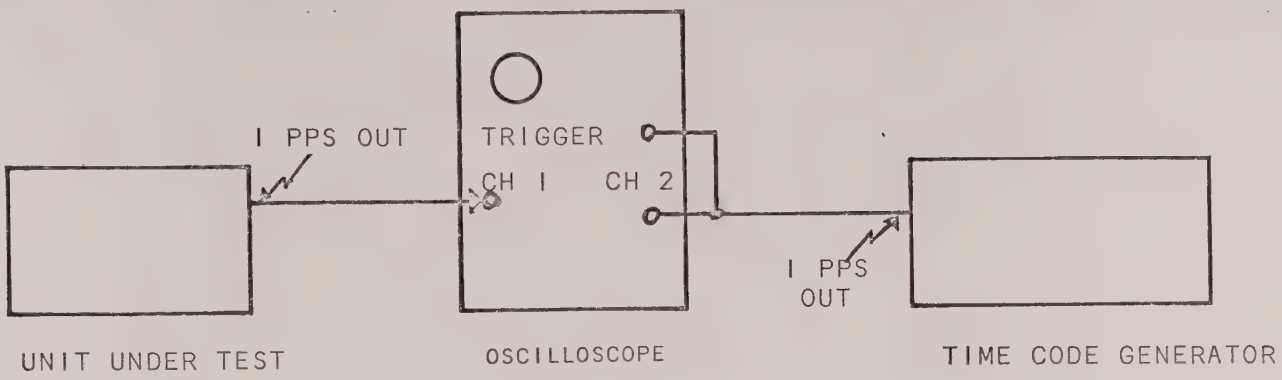


FIGURE 4-1
OSCILLATOR ACCURACY TEST

4.6.6 ADV/RET SYNCHRONIZER Dwg. 62211-7202

To test the operation of this circuit connect the oscilloscope as shown in Figure 4-2. Adjust the time base as required to give sufficient resolution for each ADV/RET rate selected.



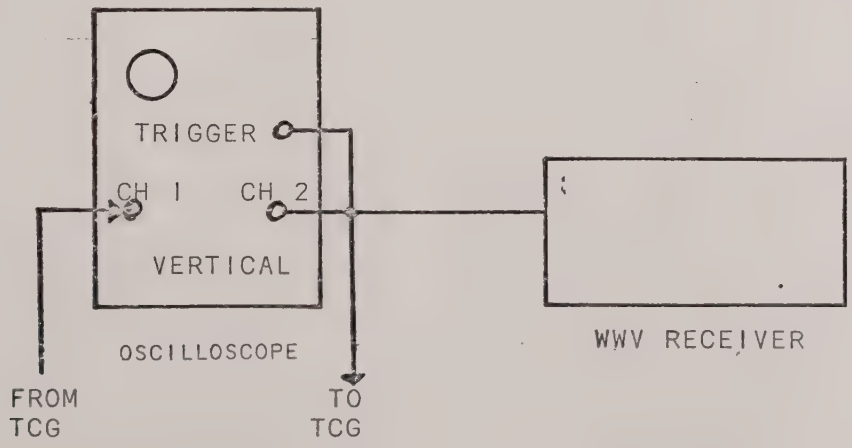
ADV/RET SYNCHRONIZER TEST

FIGURE 4-2

With both generators operating, there will be some arbitrary time difference between the pulse trains. Starting with the fastest ADV/RET rate available, verify that the pulse train from the unit under test shifts (right or left depending on whether ADV or RET is selected) the proper time increment each second. Repeat this procedure for each of the other rates. It will be necessary to bring the pulse trains into closer coincidence for each slower rate and to increase the time base speed.

4.6.7 CONTROL, INPUT/OUTPUT

To test the WWV sync circuit connect the oscilloscope as shown in Figure 4-3. Sync the scope to show the 5 cycles of 1 kHz which comprise the 1 second "TICK".



WWV SYNC CIRCUIT TEST

FIGURE 4-3

Monitor the output of the WWV sync circuit on either pin B/22 or A/15 and verify that a pulse is produced once for each burst of 1 kHz.

The code output circuit contains three adjustments. These control the shaper tuning, mark to space ratio, and nominal output amplitude.

(1) Adjust the tune (R4) control for maximum AC signal at the MOD CODE output connector.

(2) Adjust the MODE (R27) control for a nominal 3 V peak-to-peak output of the large cycle signal.

(3) Adjust the ratio (R14) control for a 3:1 modulation ratio.

(4) Readjust the tune (R6) control until the junction point of the large and small cycles has a minimum of distortion. (See Figure 4-3.)

CHAPTER 5
OVERALL FUNCTIONAL DESCRIPTION

5.1 TIME BASE ADV/RET SYNCHRONIZER

A stable 1 MHz signal is produced by the oscillator section of this card. This 1 MHz signal is divided down to 500 kHz and 100 kHz for use by the minor counters.

The ADV/RET SYNCHRONIZER allows setting the time code generator into coincidence with a standard time reference. The time may be shifted at one of six rates, 1 µs/sec to 100 ms/sec, and either advanced or retarded. Advance is accomplished by adding pulses into the minor counters, retard by deleting pulses.

5.2 TIME BASE, MINOR COUNTERS

A five decade counter divides the incoming 100 kpps signal down to 1 pps. The decades are arranged so that the first two are reset independently of the last three to permit setting of propagation delay. The EXT RESET signal resets the last three counters. RESET (and START/STOP) of the first two counters is controlled by the MANUAL or AUTO START and STOP LINES. All outputs of the decades are buffered.

Three sets of gates decode the minor counter outputs to provide square waves at 10 kHz, 1 kHz, and 100 Hz.

5.3 BCD/10 LINE DUAL DECODER

A pair of BCD to 10 line decoders decode the BCD outputs of the minor counter to provide timing signal for use by the scan gates which produce the serial ones for the output code.

5.4 CONTROL, INPUT/OUTPUT

The WWV signal used to operate the auto start circuit is processed on this card to extract the 1 second "TICK".

The code generator section of this card combines the serial ones data with the timing signals to produce a dc code.

The modulated code is generated from the dc code by amplitude modulating the output of a 1 kHz shaper. This shaper produces a 1 kHz sine wave when fed a 1 kHz signal.

5.5 ACCUMULATOR CARDS, SECONDS, MINUTES, HOURS

The accumulators store the time information and are updated by the 1 pps signal. Associated with each accumulator is a set of scan gates to produce the serial ones.

The second accumulator card contains additional circuitry to control reset and fast update (Preset).

6.1 TIME BASE/ADV-RET SYNCRHONIZER (Dwg. B62211-7202 G2)

GENERAL

The Time Base/Adv-Ret Synchronizer card performs two functions.

(1) The Time Base section generates a stable, crystal controlled 1 MHz pulse rate. This signal is divided down to 500 kpps and 100 kpps for use in the minor counters and seconds accumulator.

(2) The Advance-Retard Synchronizer section allows synchronizing the clock with an external standard. Various rates are available to facilitate precise adjustment in a minimum time.

TIME BASE

The Time Base section consists of an unheated 1 MHz crystal (Y2) operating in a Colpitts type oscillator (Q3). The resulting 1 MHz signal is applied to a clipper-amplifier, Q1. Q1 provides a 5 V p-p 1 MHz pulse rate which is buffered by A6 and applied to gate A9. Functionally, A9 is part of the Adv-Ret circuit and will be explained later. The output of gate A9 is divided by flip-flop A8 to produce both 500 kpps and 100 kpps signals. These signals are buffered for use by other circuits.

ADV-RET SYNCHRONIZER

The Adv-Ret circuit provides a means to add or subtract counts to bring the clock into coincidence with a standard time signal (Such as WWV). Six rates are provided for adding or subtracting count. Of the six, the four slowest rates are selectable with a front panel switch. The full six rates are available when the remote

control is used. Since the operation is identical at all rates, only one will be described. Rate selection is accomplished by grounding the input of the gate for the desired rate.

Refer to the Adv-Ret timing diagram, Figure 1. With the 100 ms/s rate selected, 100 kpps is applied to the clock pulse input of a flip-flop (A4-1). Since both the external J & K inputs are open (High) the output (A4-12) will change from the (Reset) zero state to the one state when the 100 kpps signal goes low. This sets the J input of another flip-flop (A4-7) high, allowing the flip-flop to change state (from zero to one) the first time the 1 MHz clock goes low. Gate A6-11 is used to reset the first flip-flop (A4-12). The output of the gate is held high whenever A4-9 is low. A reset pulse is produced the first time the 1 MHz clock goes high after A4-9 goes high. The reset pulse causes A4-12 to go low which causes A4-9 to go low the nest time the 1 MHz clock goes low. This terminates the reset pulse and completes the cycle. The cycle repeats each time the 100 kpps signal goes low, i.e. every 100 ms. In this way, 100 pulses per second are produced. Each pulse can advance or retard the clock 1 µs.

Selection of either advance or retard is accomplished by a series of gates. Two gates are connected to the input of the divider decade (A8). One (A9-3) is used to inhibit clock pulses for retard, the other (A9-6) is used to add pulses for advance. Gate A6-3 and A7-8 complete the retard selection circuit. A ground on the $\overline{\text{RET}}$ line will enable gate A7-8. This will allow flip-flop A4-9 to control gate A9-3, deleting one pulse each 100 ms.

A flip-flop (A6-8 and A5-8) and gates A7-11 and A5-6 complete the advance circuit. The flip-flop is set by a ground on the $\overline{ADV}$ line and reset every 10 ms by A5-6. When the flip-flop is set (giving a high at A6-8), gate A7-11 is enabled allowing pulses produced at A4-8 to input the divider (A8). Note that the fall time of these pulses occurs at the rise time of the 1 MHz clock out of A9-3. Therefore, an *"extra"* pulse inputs the divider (A8) each 100 ms.

This card additionally provides the non-inverted waveforms for two pulse rates used elsewhere in the unit.

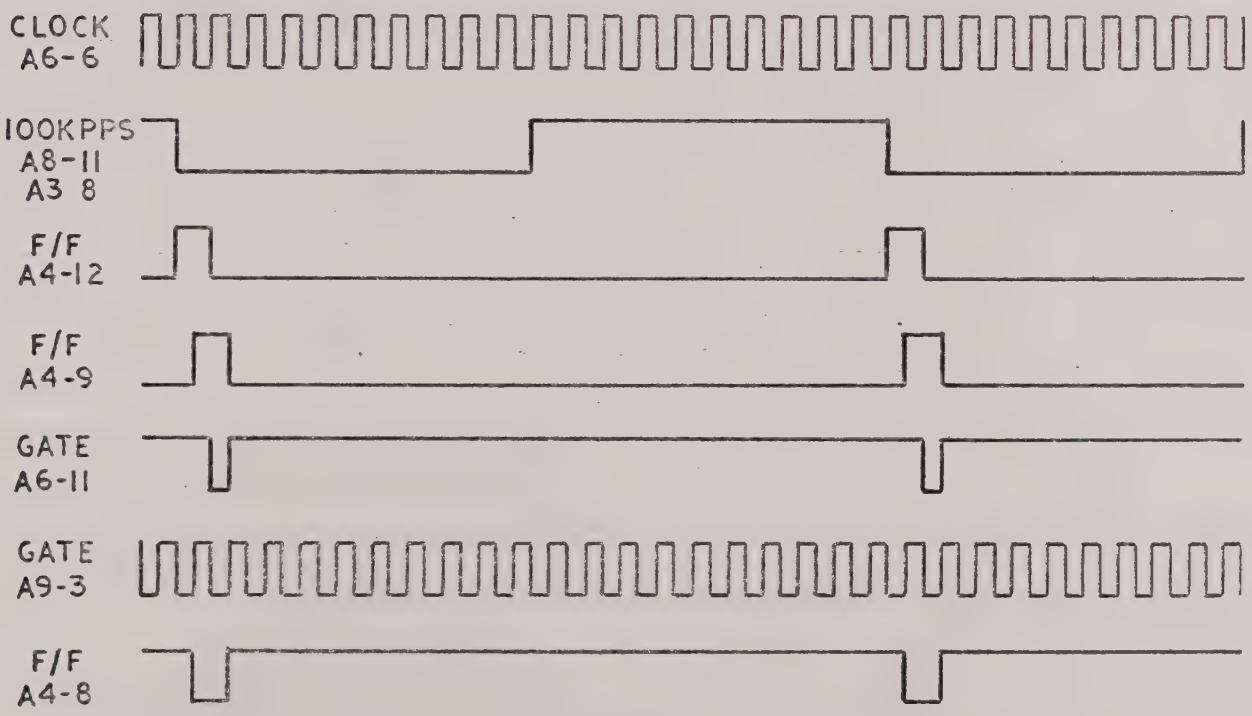


FIGURE 6.1

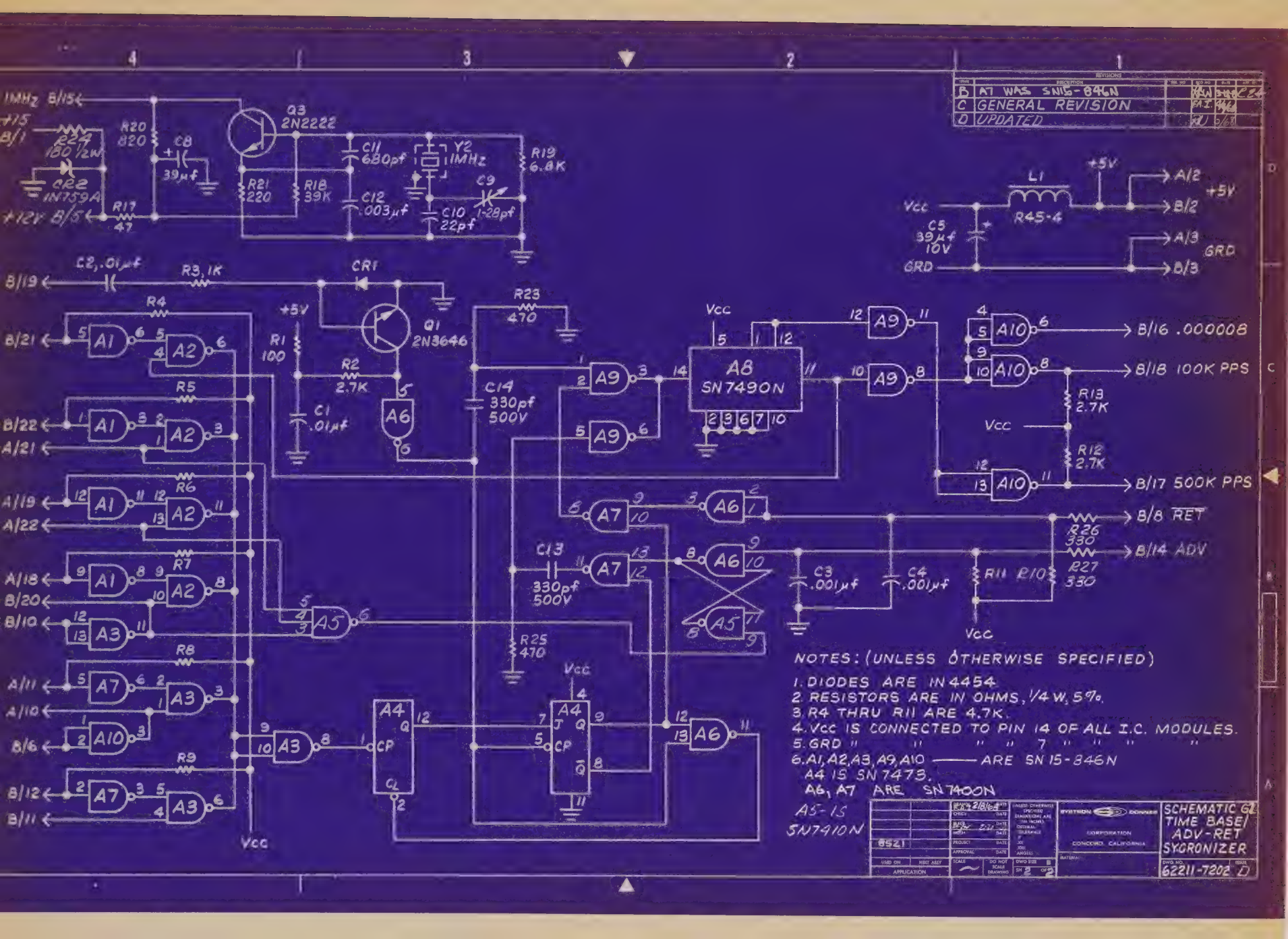
TIMING SEQUENCE
TIME BASE/ADV-RET
SYNCHRONIZER

PARTS LIST

TIME BASE/ADV-RET SYNCHRONIZER P/L 62211-8202 (G1, G2, G3)

Ref.	Description	S-D Part No.
CAPACITORS		
	Capacitor, 0.01 µf, Disc	C0233
	Capacitor, 0.001 µf, Disc	C0235
	Capacitor, 39 µf, 10 V, Tant	C0902
	Capacitor, 1-28 PF, var.	C1059 (C0555)
	Capacitor, 22 PF, Dip Mica	C0529
	Capacitor, 680 PF, Dip Mica	C0638
	Capacitor, 3000 PF, Dip Mica	C0759
	Capacitor, 330 PF, 500 V	C0540
DIODES		
	Diode, 1N4151	CR0150
	Diode, 1N759A	CR0174
INTEGRATED CIRCUITS		
	Integrated Circuit, 15-846N	I9716
	Integrated Circuit, SN7410N	I9706
	Integrated Circuit, SN7400N	I9705
	Integrated Circuit, SN7490N	I9711
	Integrated Circuit, SN7473N	I9709
TRANSISTORS		
	Transistor, 2N3646	Q0218
	Transistor, 2N2222	Q0116
RESISTORS		
	Resistor, 100 Ω, 1/4W, 5%	R0966

Ref.	Description	S-D Part No.
RESISTORS (continued)		
	Resistor, 2.7 kΩ, 1/4W, 5%	R0937
	Resistor, 1 kΩ, 1/4W, 5%	R0765
	Resistor, 4.7 kΩ, 1/4W, 5%	R0892
	Resistor, 560 Ω, 1/4 W, 5%	R0819
	Resistor, 47 Ω, 1/4 W, 5%	R0743
	Resistor, 39 kΩ, 1/4W, 5%	R0748
	Resistor, 6.8 kΩ, 1/4 W, 5%	R0696
	Resistor, 220 Ω, 1/4 W, 5%	R0760
	Resistor, 10 kΩ, 1/4W, 5%	R0766
	Resistor, 180 Ω, 1/2 W, 5%	R0725
	Resistor, 470 Ω, 1/4 W, 5%	R1044
	Resistor, 330 Ω, 1/4 W, 5%, Carbon C.	R0662
	Resistor, 820 Ω, 1/4 W, 5%	R0762
OTHER		
	Oscillator, 3 MHz (JK 013-0160)	Y0045
	Crystal, 1 MHz	Y0019
	Oscillator, 3 MHz	Y0048
	Crystal Bracket, AU6AT	H1190
	Washer, Nylon #4	H0553
	Inductor, R45-4	L0143
	Schematic	62211-7202
	Assembly	62211-4202


REVISIONS
B A7 WAS SN15-846N
C GENERAL REVISION
D UPDATED
1MHz B/15
+15 B/1
R24 180 1/2W
CR2 IN759A
+12V B/5
R17 47
R20 820
C8 39µf
Q3 2N2222
R21 220
R18 39K
C11 680pf
C12 .003µf
Y2 1MHz
C9 1-28pf
C10 22pf
R19 6.8K
L1
R45-4
+5V
Vcc
C5 39µf 10V
GRD
A/2
B/2
A/3
B/3
+5V
GRD
B/19
C2, .01µf
R3, 1K
CR1
Q1 2N3646
R1 100
R2 2.7K
C1 .01µf
R4
R5
R6
R7
R8
R9
B/21
B/22
A/21
A/19
A/22
A/18
B/20
B/10
A/11
A/10
B/6
B/12
B/11
A1
A2
A3
A5
A6
A7
A10
+5V
R23 470
C14 330pf 500V
R25 470
C13 330pf 500V
A8 SN7490N
A9
Vcc
C3 .001µf
C4 .001µf
R11 R10
R13 2.7K
R12 2.7K
R26 330
R27 330
B/16 .000008
B/18 100K PPS
B/17 500K PPS
B/8 RET
B/14 ADV
A4 Q CP CL
A4 J Q CP Q
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. DIODES ARE IN4454
2. RESISTORS ARE IN OHMS, 1/4 W, 5%.
3. R4 THRU R11 ARE 4.7K.
4. Vcc IS CONNECTED TO PIN 14 OF ALL I.C. MODULES.
5. GRD " " " 7 " " " "
6. A1, A2, A3, A9, A10 —— ARE SN 15-846N
A4 IS SN 7473.
A6, A7 ARE SN 7400N
A5 IS SN 7410N
8521
SCHEMATIC GL TIME BASE/ ADV-RET SYGRONIZER
DWG NO. 62211-7202
ISSUE D

6.2 TIME BASE/MINOR COUNTERS (Dwg. B62112-7502 G1, G2, G3)

GENERAL

This card is basically a five decade counter with start/stop gating, reset, and buffered outputs. Logic is also provided to generate square waves at 10 kHz, 1 kHz, and 100 Hz.

START/STOP

The first two decades of the divider are isolated from the remaining three decades to permit presetting propagation delay into the unit when the remote control is used. In this case jumpers W2 and W3 are connected in the alternate configuration, preventing A12 and A10 from resetting when a stop command occurs.

Flip-flop A13 provides a reset signal under two different conditions. A ground on the $\overline{\text{MAN STOP}}$ line will unconditionally set A13 in the stop condition, providing reset. A ground on the $\overline{\text{STOP}}$ line will permit A13 to go to the stop condition the first time the auto stop line goes low. The auto stop line has a negative spike once per second, on time. Removal of the reset signal occurs unconditionally when any of three conditions are satisfied. 1) Ground on the $\overline{\text{RUN}}$ line, 2) Ground on the $\overline{\text{AUTO START}}$ line, or 3) A high on the EXT START line. Transistor Q2 is used as an inverter and a gate for the various start commands. Transistor Q1 is used to remove the input signal to the decade counters during stop to preserve the count in A12 and A10 when using the remote control.

DECADE COUNTERS

Five decade counters are connected to divide by incoming 100 kpps

signal down to 1 pps. Each of the outputs from the decades is buffered and brought out to a pin in an inverted condition. In addition, two outputs (8×10^{-5} and 8×10^{-4}) are double buffered to provide the non-inverted condition. Reset for the last three decades is provided via transistor Q3 when a ground is present on the $\overline{\text{EXT RESET}}$ line.

SQUARE WAVE OUTPUTS

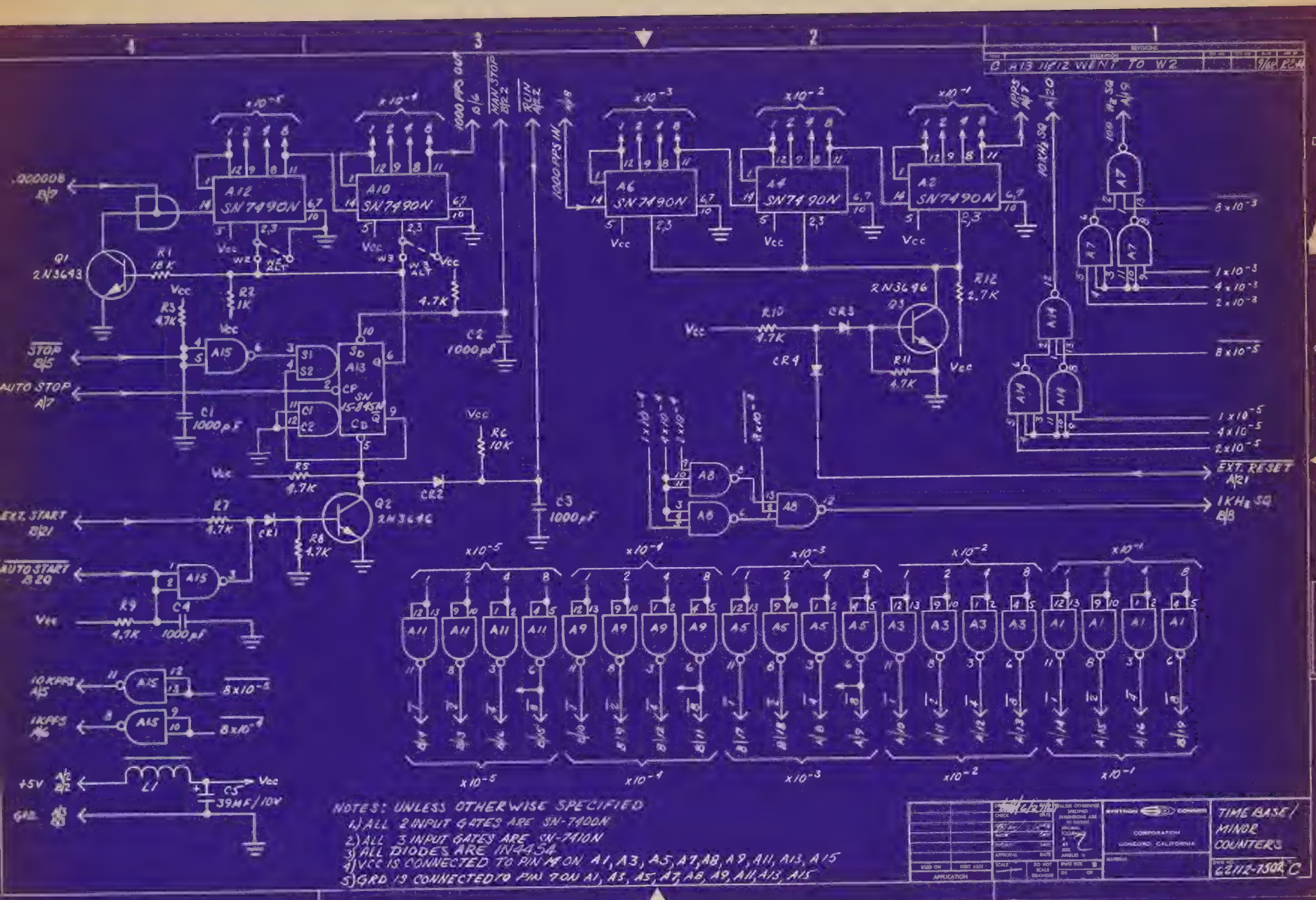
Three square wave signals are provided by this card. Gates A14 decode sufficient lines to give a 10 kHz square wave. Gates A8 yield 1 kHz and gates A7, 100 Hz.

PARTS LIST

TIME BASE/MINOR COUNTER P/L 62112-8502 (G1, G2, G3, G4)

Ref.	Description	S-D Part No.
CAPACITORS		
C1-4	Capacitor, 1000 pf	C0543
C5	Capacitor, 39 µf, 10 V	C0902
DIODES		
CR1-5	Diode, 1N4151	CR0150
INTEGRATED CIRCUITS		
A1, 3, 5, 9, 11	Integrated Circuit, SN7400N	19705
A2, 4, 6, 10, 12	Integrated Circuit, SN7490N	19711
A7, 8, 14	Integrated Circuit, SN7410N	19706
A13	Integrated Circuit, SN15-845N	19715
TRANSISTORS		
Q1	Transistor, 2N3643	Q0179
Q2-3	Transistor, 2N3646	Q0218
RESISTORS		
R1	Resistor, CC, 18 kΩ, 1/4 W, 5%	R0785
R2	Resistor, 1 kΩ, 1/4 W, 5%, CC	R0765
R3-5, 7-11	Resistor, 4.7 kΩ, 1/4 W, 5%, CC	R0892
R6	Resistor, 10 kΩ, 1/4 W, 5%, CC	R0766
R12	Resistor, 2.7 kΩ, 1/4 W, 5%, CC	R0937
OTHER		
L1	Inductor, R45-4	L0143

Ref.	Description	S-D Part No.
OTHER (continued)		
	Schematic	62112-7502
	Assembly	62112-4502


REVISIONS
C A13 J1F12 WENT TO W2
A12 SN7490N
A10 SN7490N
A6 SN7490N
A4 SN7490N
A2 SN7490N
Q1 2N3643
Q2 2N3640
Q3 2N3646
A13 SN7545N
R1 18K
R2 1K
R3 4.7K
R4 4.7K
R5 4.7K
R6 4.7K
R7 4.7K
R8 4.7K
R9 4.7K
R10 4.7K
R11 4.7K
R12 2.7K
RC 10K
C1 1000 pF
C2 1000 pF
C3 1000 pF
C4 1000 pF
C5 39MF/10V
CR1
CR2
CR3
CR4
L1
1000 PPS OUT
MAN STOP
RUN
1000 PPS IN
10 KPPS OUT
10 KPPS IN
1KPPS OUT
100 PPS OUT
STOP
AUTO STOP
EXT. START
AUTO START
EXT. RESET
1KHz SQ
+5V
GRD
Vcc
NOTES: UNLESS OTHERWISE SPECIFIED
1) ALL 2 INPUT GATES ARE SN-7400N
2) ALL 3 INPUT GATES ARE SN-7410N
3) ALL DIODES ARE IN4454
4) VCC IS CONNECTED TO PIN 14 ON A1, A3, A5, A7, A8, A9, A11, A13, A15
5) GRD IS CONNECTED TO PIN 7 ON A1, A3, A5, A7, A8, A9, A11, A13, A15
SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
TIME BASE / MINOR COUNTERS
DWG NO. 22112-1508 C

6.3 BCD TO LINE DUAL DECODER (Dwg. B62211-7201 G1)

GENERAL

This card contains two BCD to decimal converters plus necessary inverters. In addition three control lines have circuitry on the card. The decimal outputs provide timing signals for serial readout of the time accumulators.

BCD TO DECIMAL CONVERTER

The operation of both converters is identical, therefore only one will be described. The converter uses 16-two input gates to decode a standard 1-2-4-8 BCD signal into straight 10 line decimal. In addition three gates are used as inverters for the $\overline{1}$, $\overline{2}$, $\overline{4}$ incoming lines.

CONTROL LINE CIRCUITS

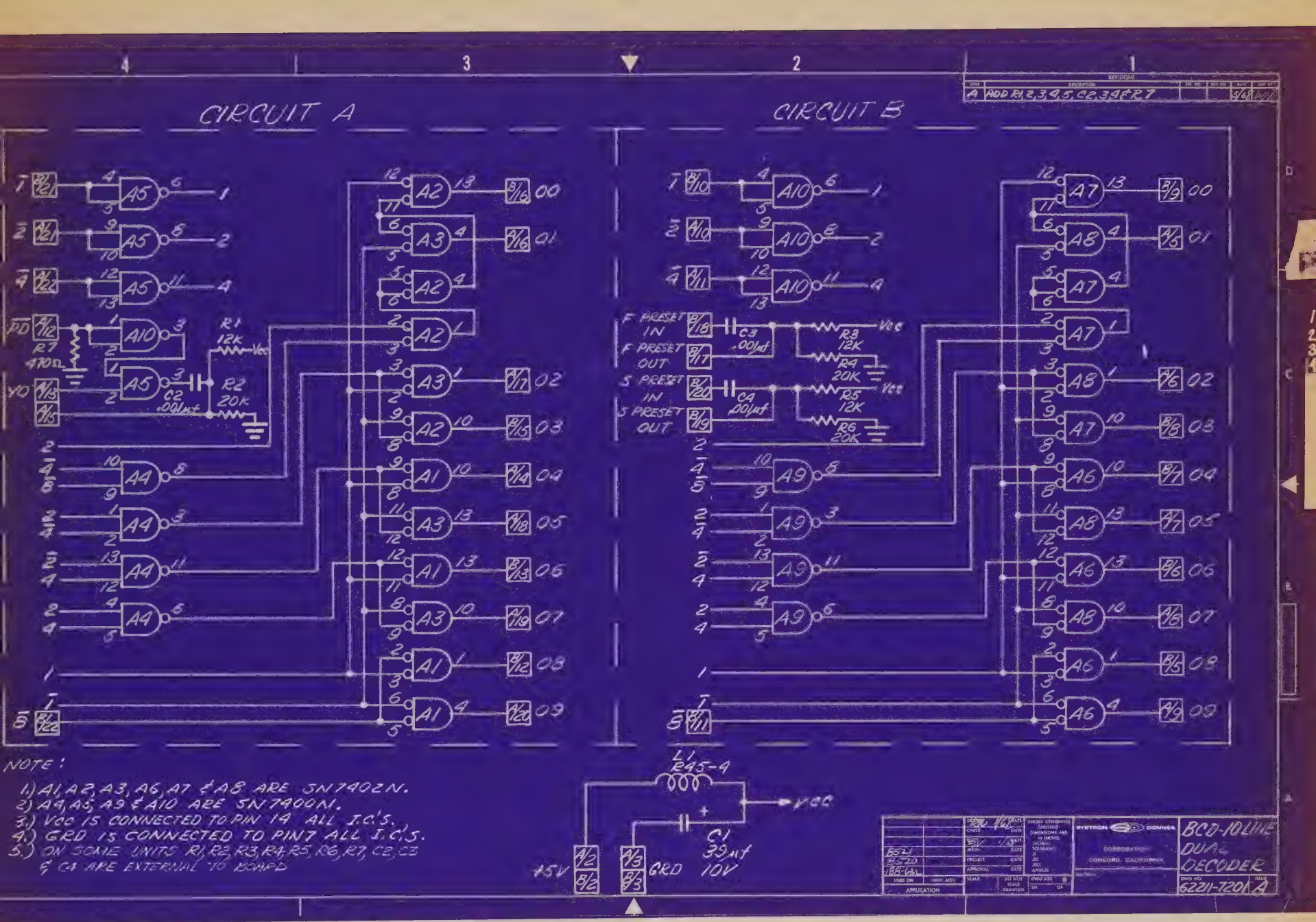
The auto stop signal is generated from the "zero" output (Y0, specifically) of the converter. This output occurs once per second and lasts 100 ms. As RC network (R1, R2, C2) transforms the pulse into a negative going spike (at the leading edge). Gate A5-3 and inverter A10-3 permit a high on the $\overline{\text{PROP. DELAY}}$ line to inhibit the auto stop signal. This signal is provided by the remote control unit.

Two different present signals are provided from this card. The fast preset is at a 5 pps rate and is derived from the $\overline{1}$ bit and is shaped by RC network R3, R4, C3 into a series of spikes. The slow preset comes from the $\overline{8}$ bit and is similarly shaped by R5, R6, C4.

PARTS LIST

BCD 10 LINE DUAL DECODER P/L 62211-8201 (G1)

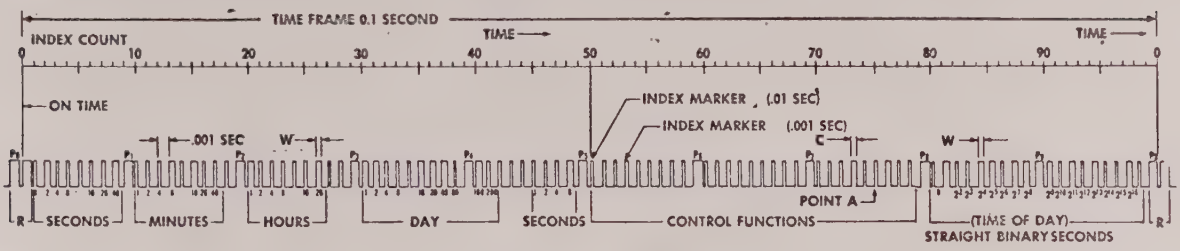
Ref.	Description	S-D Part No.
CAPACITORS		
	Capacitor, 39 µf, 10 V	C0902
	Capacitor, 0.001 µf, 1000 V	C0235
INTEGRATED CIRCUITS		
	Integrated Circuit, SN7400N	19705
	Integrated Circuit, SN7402N	25709
RESISTORS		
	Resistor, CC, 12 kΩ, 1/4 W, 5%	R0759
	Resistor, CC, 20 kΩ, 1/4 W, 5%	R0964
	Resistor, CC, 470 Ω, 1/4 W, 5%	R1044
OTHER		
	Inductor, R45-4	L0143
	Schematic	B62211-7201
	Assembly	62211-4201


CIRCUIT A
CIRCUIT B
REVISIONS
A ADD R1,2,3,4,5, C2,3 & F27
R1 12K
R2 20K
C2 .001mf
R7 470Ω
C3 .001mf
R3 12K
R4 20K
C4 .001mf
R5 12K
R6 20K
F PRESET IN
F PRESET OUT
S PRESET IN
S PRESET OUT
Vcc
L1 E45-4
C1 39mf 10V
+5V
GRD
NOTE:
1.) A1, A2, A3, A6, A7 & A8 ARE SN7402N.
2.) A4, A5, A9 & A10 ARE SN7400N.
3.) Vcc IS CONNECTED TO PIN 14 ALL I.C.'S.
4.) GRD IS CONNECTED TO PIN 7 ALL I.C.'S.
5.) ON SCALE UNITS R1, R2, R3, R4, R5, R6, R7, C2, C3 & C4 ARE EXTERNAL TO BOARD
BYETRON CONVER CORPORATION CONCORD, CALIFORNIA
BCD-10 LINE DUAL DECODER
DWG NO. 62211-7201 A

IRIG TIME CODE FORMATS

FORMAT A

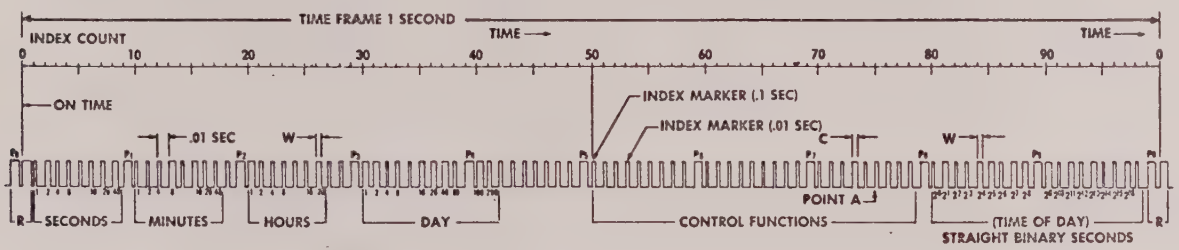
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:18:42 + .8 + .07 + .005 21 HR. 18 MIN. 42.875 SEC. ON DAY 173

FORMAT B

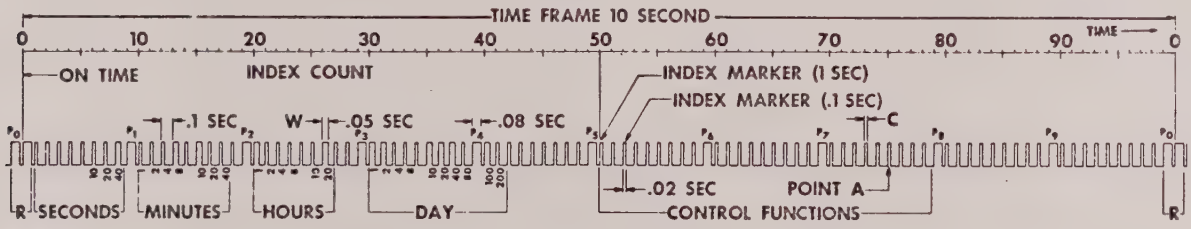
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:18:42 + .7 + .05 = 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

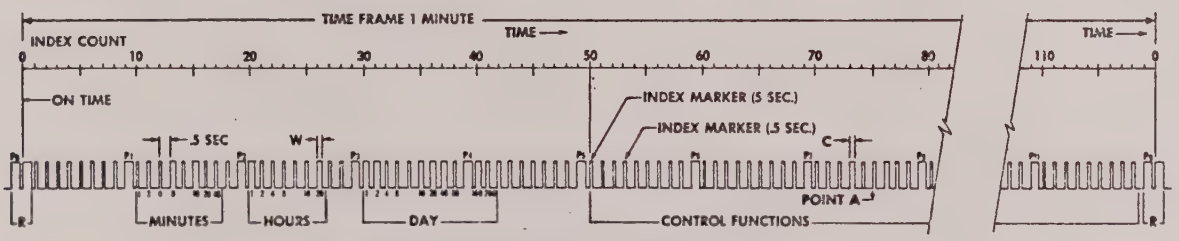
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A = 21:18:40 + 7 + .5 = 21 HR. 18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

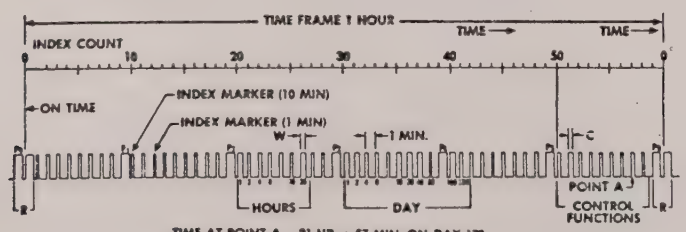
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



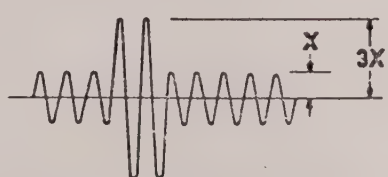
TIME AT POINT A = 21:18 + 37.5 SEC. = 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE



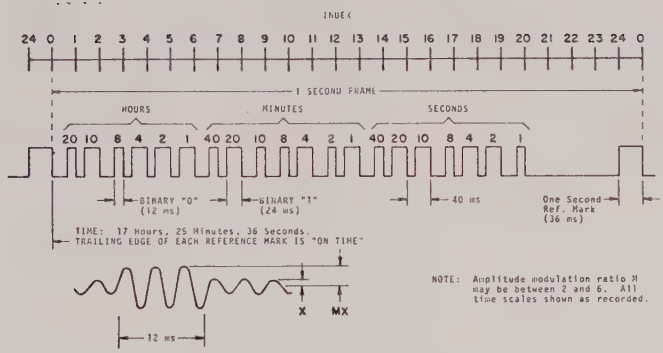
TIME AT POINT A = 21 HR. + 57 MIN. ON DAY 173



TYPICAL MODULATED SIGNAL

OPTIONAL CODES
and
CODE FORMATS

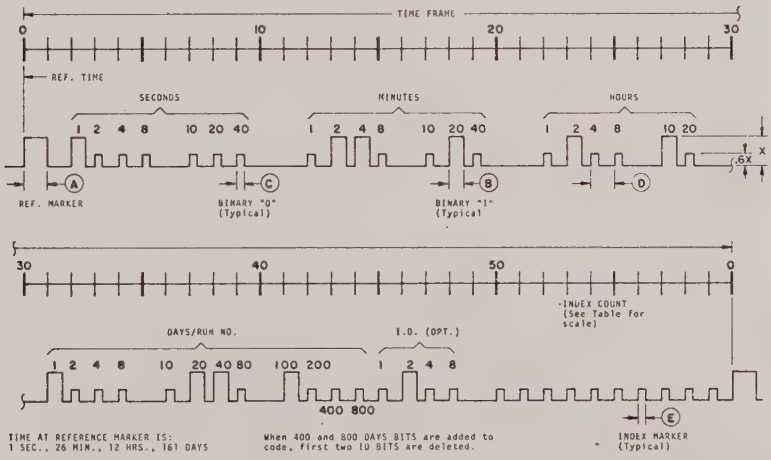
XR 3 TIME CODE FORMAT


INDEX
24 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 0
1 SECOND FRAME
HOURS
MINUTES
SECONDS
20 10 8 4 2 1 40 20 10 8 4 2 1 40 20 10 8 4 2 1
BINARY "0" (12 ms)
BINARY "1" (24 ms)
40 ms
One Second Ref. Mark (36 ms)
TIME: 17 Hours, 25 Minutes, 36 Seconds.
TRAILING EDGE OF EACH REFERENCE MARK IS "ON TIME"
X
MX
12 ms
NOTE: Amplitude modulation ratio M may be between 2 and 6. All time scales shown as recorded.

TYPICAL MODULATED CODE ELEMENT "ZERO" (250 Hz Carrier)

For 1 kHz carrier large amplitude cycles number 12, 24, and 36

SLOW CODE -- TYPE "B"



TIME AT REFERENCE MARKER IS: 1 SEC., 26 MIN., 12 HRS., 161 DAYS

When 400 and 800 DAYS BITS are added to code, first two IU BITS are deleted.

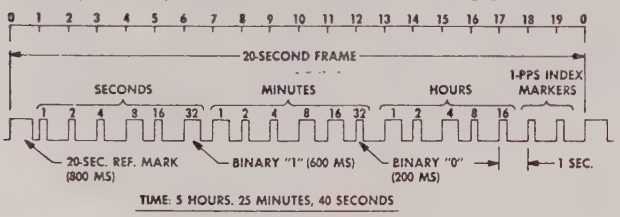
Pulse Rate	Time Frame	D-Period	A-Width	B-Width	C-Width	E-Width	Number of Pulses in Time Frame
1. 50	1 SEC	20 ms	20 ms	10 ms	4 ms	4 ms	50
2. 10	5 SEC	100 ms	100 ms	50 ms	20 ms	20 ms	50
3. 5	10 SEC	200 ms	200 ms	100 ms	40 ms	40 ms	50
4. 2	30 SEC	1/2 SEC	1/2 SEC	250 ms	100 ms	100 ms	60
5. 1	60 SEC	1 SEC	1 SEC	1/2 SEC	200 ms	200 ms	60
6. 1/2	5 MIN	5 SEC	5 SEC	2-1/2 SEC	1 SEC	1 SEC	60
7. 1/10	10 MIN	10 SEC	10 SEC	5 SEC	2 SEC	2 SEC	60
8. 2 ppm	30 MIN	30 SEC	30 SEC	10 SEC	6 SEC	5 SEC	60
9 1 ppm	60 MIN	60 SEC	60 SEC	30 SEC	12	12 SEC	60

OPTIONAL CODES
and
CODE FORMATS

AMR TIME CODE FORMATS

ATLANTIC MISSILE RANGE NO. B1

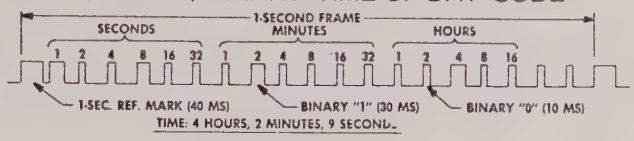
17-BIT, 1-PPS, BINARY TIME-OF-DAY CODE


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 0
20-SECOND FRAME
SECONDS
MINUTES
HOURS
1-PPS INDEX MARKERS
1 2 4 8 16 32 1 2 4 8 16 32 1 2 4 8 16
20-SEC. REF. MARK (800 MS)
BINARY "1" (600 MS)
BINARY "0" (200 MS)
1 SEC.

TIME: 5 HOURS, 25 MINUTES, 40 SECONDS

ATLANTIC MISSILE RANGE NO. C1

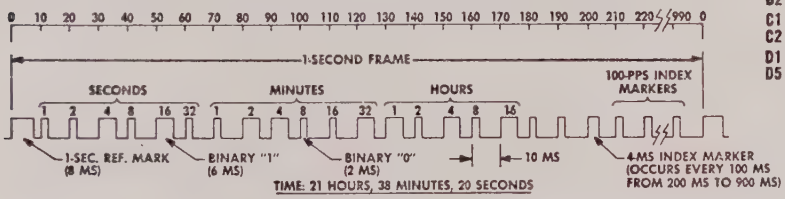
17-BIT, 20-PPS, BINARY TIME-OF-DAY CODE



TIME: 4 HOURS, 2 MINUTES, 9 SECONDS

ATLANTIC MISSILE RANGE NO. D1

17-BIT, 100-PPS, BINARY TIME-OF-DAY CODE

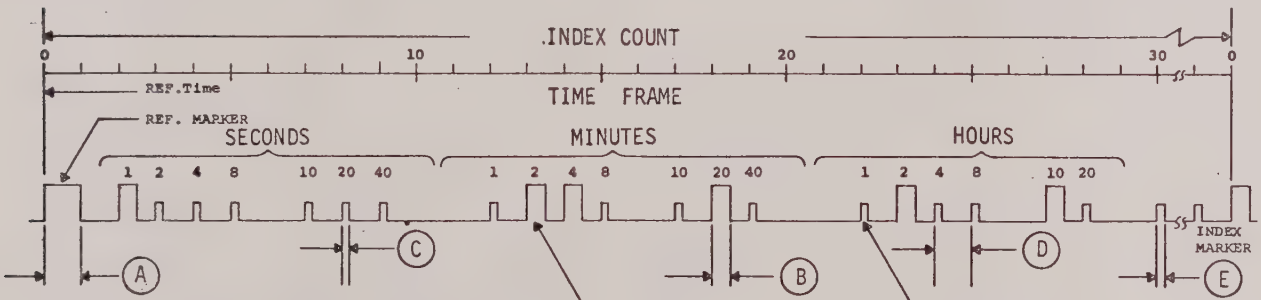

0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180 190 200 210 220 990 0
1-SECOND FRAME
SECONDS
MINUTES
HOURS
100-PPS INDEX MARKERS
1 2 4 8 16 32 1 2 4 8 16 32 1 2 4 8 16
1-SEC. REF. MARK (8 MS)
BINARY "1" (6 MS)
BINARY "0" (2 MS)
10 MS
4-MS INDEX MARKER (OCCURS EVERY 100 MS FROM 200 MS TO 900 MS)

TIME: 21 HOURS, 38 MINUTES, 20 SECONDS

AMR SIGNAL DESIGNATIONS

AMR NO.	17-BIT, 24-HOUR BINARY CODE
B1	1 PPS (pulse width)
B2	1 PPS (modulated)
C1	20 PPS (pulse width)
C2	20 PPS (modulated)
D1	100 PPS (pulse width)
D5	100 PPS (modulated)

SLOW CODE - TYPE 'A'



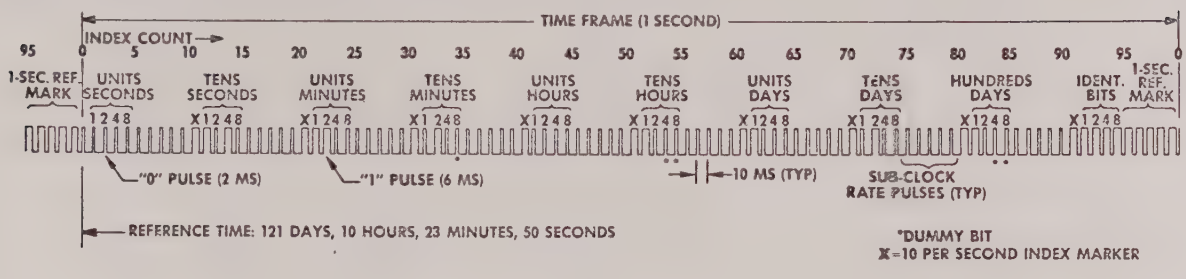
	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec.	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs.	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs.	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs.	1 Sec.	1 Sec.	500 ms	200 ms	200 ms	30
5	1/2 pps	60 Secs.	2 Secs.	2 Secs.	1 Sec.	400 ms	400 ms	30
6	1/10 pps	5 Mins.	10 Secs.	10 Secs.	5 Secs.	2 Secs.	2 Secs.	30
7	1/20 pps	10 Mins.	20 Secs.	20 Secs.	10 Secs.	4 Secs.	4 Secs.	30
8	1 ppm	30 Mins.	1 Min.	1 Min.	30 Secs.	12 Secs.	12 Secs.	30
9	1/2 ppm	60 Mins.	2 Mins.	2 Mins.	1 Min.	24 Secs.	24 Secs.	30

REFERENCE MARKER = 100% OF PERIOD
BINARY "1" = 50% OF PERIOD
BINARY "0" = 20% OF PERIOD
BINARY "1" AMPLITUDE = + 10V DC
BINARY "0" AMPLITUDE = + 6V DC

NASA TIME CODE FORMATS

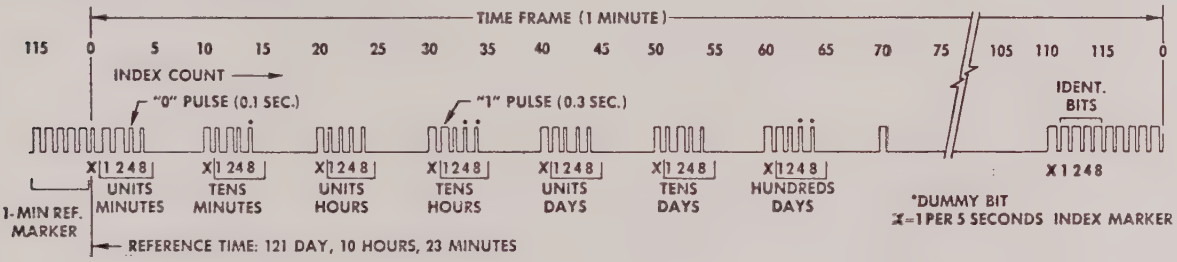
36-BIT, 100-PPS CODE (1000-CPS CARRIER)

SHOWING SUB-CLOCK RATE PULSES



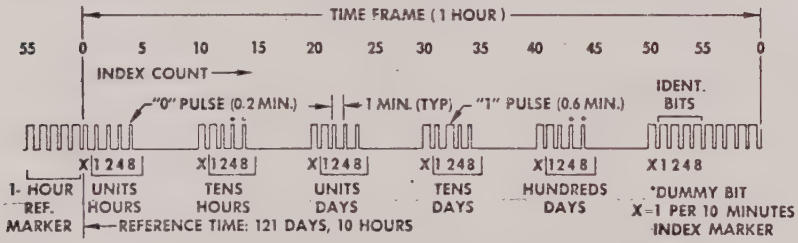
28-BIT, 2-PPS CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED

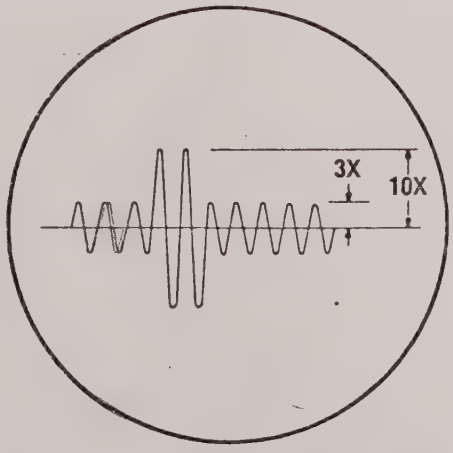

TIME FRAME (1 MINUTE)
115 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 105 110 115 0
INDEX COUNT
"0" PULSE (0.1 SEC.)
"1" PULSE (0.3 SEC.)
IDENT. BITS
X 1 2 4 8
1-MIN REF. MARKER
UNITS MINUTES
TENS MINUTES
UNITS HOURS
TENS HOURS
UNITS DAYS
TENS DAYS
HUNDREDS DAYS
X 1 2 4 8
*DUMMY BIT
X=1 PER 5 SECONDS INDEX MARKER
REFERENCE TIME: 121 DAY, 10 HOURS, 23 MINUTES

20-BIT, 1-PPM CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED



Insertion of sub-clock rate pulses is controlled for each format by individual control switches.



TYPICAL MODULATED SIGNAL

OPTIONAL CODES
and
CODE FORMATS

6.4 SECONDS ACCUMULATOR (Dwg. 62112-7504 GI)

GENERAL

This card contains circuitry to totalize the 1 pps signal and give a readout (1-2-4-8 Binary) in units & tens of seconds. Scan gates are provided to give serial ones. Additional circuitry controls reset and fast update.

FAST UPDATE CIRCUIT

When the REMOTE CONTROL unit is used with the unit, provision is made for serially updating all the accumulators. Switches on the remote control unit set the time to be preset and a signal is sent by the remote to indicate that the accumulators are in coincidence with the preset switches this causes the update to stop. Flip-flop A12 provides a fast update enable signal under proper conditions. This signal allows a 100 kpps signal to input the accumulators in place of the normal 1 pps. Gates A7-3 and A7-6 perform the selection.

A number of conditions must be present to allow the fast update to preset the accumulators. The $\overline{\text{PRESET TIME}}$ line must be grounded. This signal is open (High) when either *"Start"* or *"Run"* modes are selected. With the $\overline{\text{PRESET TIME}}$ line open, transistor Q1 will be turned on, holding A12 in a clear condition and preventing fast update. Also, even with the $\overline{\text{PRESET TIME}}$ line at ground, a reset command will turn Q1 on via the wired OR. Assuming Q1 is off, fast update is initiated by a ground on the $\overline{\text{TIME PRESET}}$ line (Pin B/4). Note that a preset time signal (This is $\overline{\text{PRESET TIME}}$ inverted by A13-6) is used to hold off the $\overline{\text{TIME PRESET}}$ at the

same time that A12 is held in a clear condition. A one shot (A13-3 and A13-11) pulses the steering gates of A12 to start the update. The preset time signal is again used at this point. When the accumulators reach the same number that was preset, a ground on the $\overline{\text{COINC. TIME}}$ line from the remote control unit is inverted by A7-11 and shuts off the fast update. Note that the $\overline{\text{PRESET TIME}}$ signal is used to disable the 1 pps input except in Start and Run modes via R15, C8, and R16.

RESET CIRCUIT

Reset for all the accumulators is initiated by a ground on Pin B/5, $\overline{\text{TIME RESET}}$. Again, the preset time signal is used to prevent reset via the $\overline{\text{TIME RESET}}$ line when in start or run modes. An $\overline{\text{EXT RESET}}$ line (Pin A/6) is available which will always supply a reset command. A one shot A6-12 and A6-6, plus inverter A6-8 provide a 250 μs pulse for reset.

ACCUMULATOR CIRCUIT

The gated 1 pps signal is fed to two dividers, A2 and A9, A2 divides by ten, A9 by six. BCD is provided from each divider as well as a 1 ppm pulse for the hours accumulator. Each output is double buffered with both the inverted and non-inverted outputs brought out.

SCAN GATES

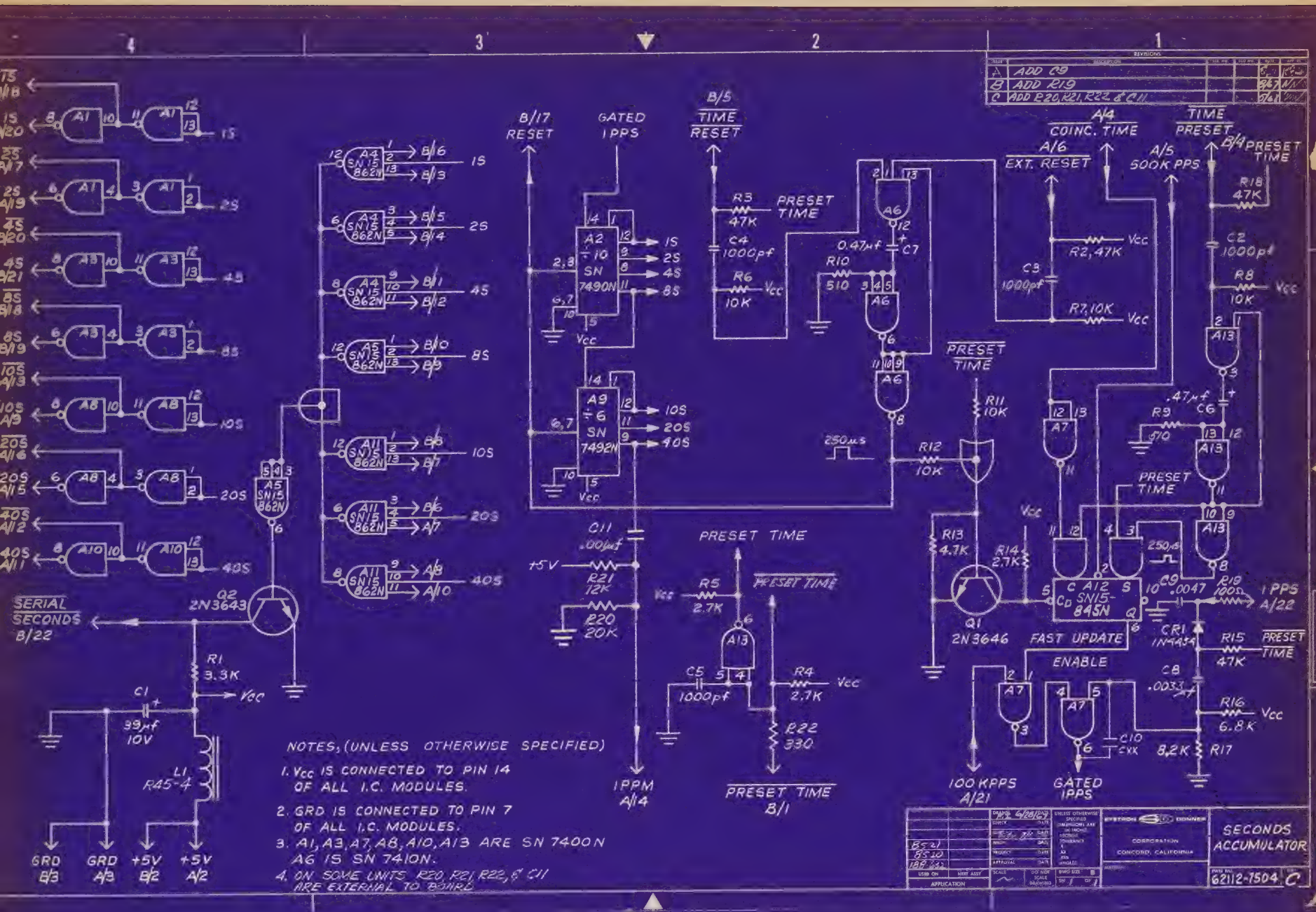
$\overline{\text{SERIAL SECONDS}}$ is produced by sequentially gating each output line into transistor Q2. Each of the three input scan gates has two timing signals and one output line applied to it. The timing signals cause each output to be read at the proper time and therefore produces a serial output.

PARTS LIST

SECONDS ACCUMULATOR P/L 62112-8504 (G1 and G3)

Ref.	Description	S-D Part No.
CAPACITORS		
	Capacitor, 39 µf, 10 V	C0902
	Capacitor, 0.001 µf, DM15	C0543
	Capacitor, 0.47 µf, 20 V, Tant	C0733
	Capacitor, 0.0047 µf, 200 V	C0698
	Capacitor, 68 pf, DM15	C0635
	Capacitor, 0.0033 µf, 200 V	C0774
	Capacitor, 0.001 µf, 1000 V	C0235
DIODES		
	Diode, 1N4151	CR0150
INTEGRATED CIRCUITS		
	Integrated Circuit, SN7400N	19705
	Integrated Circuit, SN7490N	19711
	Integrated Circuit, SN15-862N	19719
	Integrated Circuit, SN7410N	19706
	Integrated Circuit, SN7492N	23442
	Integrated Circuit, SN15-845N	19715
TRANSISTORS		
	Transistor, 2N3646	Q0218
	Transistor, 2N4124	Q0235
RESISTORS		
	Resistor, 470 kΩ, 1/4 W, 5%	R1060
	Resistor, 47 kΩ, 1/4 W, 5%	R0777

Ref.	Description	S-D Part No.
RESISTORS (continued)		
	Resistor, 10 kΩ, 1/4 W, 5%, CC	R0766
	Resistor, 2.7 kΩ, 1/4 W, 5%, CC	R0937
	Resistor, 510 Ω, 1/4 W, 5%, CC	R0984
	Resistor, 4.7 kΩ, 1/4 W, 5%, CC	R0892
	Resistor, 6.8 kΩ, 1/4 W, 5%, CC	R0696
	Resistor, 8.2 kΩ, 1/4 W, 5%, CC	R0883
	Resistor, 3.3 kΩ, 1/4 W, 5%, CC	R0742
	Resistor, 100 Ω, 1/4 W, 5%, CC	R0966
	Resistor, 20 kΩ, 1/4 W, 5%, CC	R0964
	Resistor, 12 kΩ, 1/4 W, 5%, CC	R0759
	Resistor, 330 Ω, 1/4 W , 5%, CC	R0662
OTHER		
	Choke	L0143
	Schematic	62112-7504
	Assembly	62112-4504


REVISIONS
A ADD C9
B ADD R19
C ADD R20, R21, R22 & C11
B/17 RESET
GATED 1 PPS
B/5 TIME RESET
A/4 COINC. TIME
A/6 EXT. RESET
A/5 500K PPS
TIME PRESET
B/4 PRESET TIME
PRESET TIME
R3 47K
C4 1000pf
R6 10K
R10 510
0.47μf C7
R2, 47K
C9 1000pf
R7, 10K
R18 47K
C2 1000pf
R8 10K
R11 10K
R12 10K
250μs
R13 4.7K
R14 2.7K
R9 470
.47μf C6
C11 .001μf
+5V
R21 12K
R20 20K
R5 2.7K
C5 1000pf
R4 2.7K
R22 330
C9 .0047
R10 100Ω
1 PPS A/22
CR1 IN4454
R15 47K
C8 .0033μf
R16 6.8K
R17 8.2K
C10 ±XX
SERIAL SECONDS B/22
Q2 2N3643
Q1 2N3646
FAST UPDATE ENABLE
100 KPPS A/21
GATED 1PPS
1PPM A/14
PRESET TIME B/1
R1 3.3K
C1 39μf 10V
L1 R45-4
GRD B/3
GRD A/3
+5V B/2
+5V A/2
NOTES, (UNLESS OTHERWISE SPECIFIED)
1. Vcc IS CONNECTED TO PIN 14 OF ALL I.C. MODULES.
2. GRD IS CONNECTED TO PIN 7 OF ALL I.C. MODULES.
3. A1, A3, A7, A8, A10, A13 ARE SN 7400 N A6 IS SN 7410N.
4. ON SOME UNITS R20, R21, R22, & C11 ARE EXTERNAL TO BOARD
SECONDS ACCUMULATOR
62112-7504 C

6.5 MINUTES ACCUMULATOR (Dwg. B621-12-7505 G1)

GENERAL

This card produces the minutes readout in both parallel and serial form.

ACCUMULATOR CIRCUIT

Two dividers, A9 and A7, are used to first divide the 1 ppm signal by 10 and then by 6, producing a 1 pph signal. BCD signals are double buffered with both the inverted and non-inverted outputs brought out. Reset is provided for each divider.

SCAN GATES

$\overline{\text{SERIAL MINUTES}}$ is produced by sequentially gating each output line into transistor Q1. Each of the three input scan gates has two timing signals and one output line applied to it. The timing signals cause each output to be read at the proper time and therefore produces a serial output.

ACCUMULATORS (G1, G2, G3, G4) (Dwg. 62112-8505 G1, G2, G3, G4)

Ref.	Description	S-D Part No.
CAPACITORS		
C1	Capacitor, 39 µf, 10 V	C0902
C2	Capacitor, 0.47 µf, 35VV	C0733
C3	Capacitor, 1000 pf	C0543
C4	Capacitor, 1000 pf	C0543
C5	Capacitor, 0.001 µf, Disc	C0235
C6	Capacitor, 0.001 µf, Disc	C0235
C7	Capacitor, 470 pf, Mica	C0542
C8	Capcitor, CXXXX DM-15	
INTEGRATED CIRCUITS		
A1,55, 8, 10, 11	Integrated Circuit, SN7400N	19705
A4	Integrated Circuit, SN7410N	19706
A3, 9	Integrated Circuit, SN7490N	19711
A7	Integrated Circuit, SN7492N	23442
A2, 6, 12	Integrated Circuit, SN15-862N	19719
TRANSISTORS		
Q1	Transistor, 2N3643	Q0179
RESISTORS		
R1	Resistor, CC, 470 Ω, 1/4 W, 5%	R1044
R2	Resistor, CC, 3.3 kΩ, 1/4 W, 5%	R0742
R3, 5	Resistor, 12 kΩ , 1/4 W, 5%	R0759
R4	Resistor, CC, 20 kΩ, 1/4 W, 5%	R0964
R6	Resistor, CC, 330 Ω, 1/4 W, 5%	R0662

ACCUMULATOR (G1, G2, G3, G4)
P/L 62112-8505 G1, G2, G3, G4
CONTINUED

Ref.	Description	S-D Part No.
RESISTORS (continued)		
R7	Resistor, CC, 20 kΩ, 1/4 W, 5%	R0964
OTHER		
L1	Inductor, R45-4	L0143
	Schematic	B62112-7505
	Assembly	B62112-4505

6.6 HOURS ACCUMULATOR (Dwg. B62112-7505 G2 & G4)

GENERAL

This card provides hours readout in both parallel and serial form. Additional circuitry is provided to allow selection of 24 (G2) or 48 (G4) hour recycle time.

RECYCLE CIRCUIT

The hours accumulator may be reset to zero either by the internal reset signal on Pin A/11, via gate A10 and one shot A4, or by one of two AND gates. One of these gates, when C3 is connected, will provide a pulse to one shot A4 when the counter reaches 24 hours, resetting the counter to zero. The other gate, via C4, performing reset at 48 hours.

ACCUMULATOR CIRCUIT

Two decade counters A9 and A3 divide the 1 pph input signal down until recycle occurs at either 24 or 48 hours. An output signal for a days counter may be taken from either a "20" or "40" output, depending on the recycle time selected. The BCD outputs are double buffered with both the inverted and non-inverted outputs brought out.

SCAN GATES

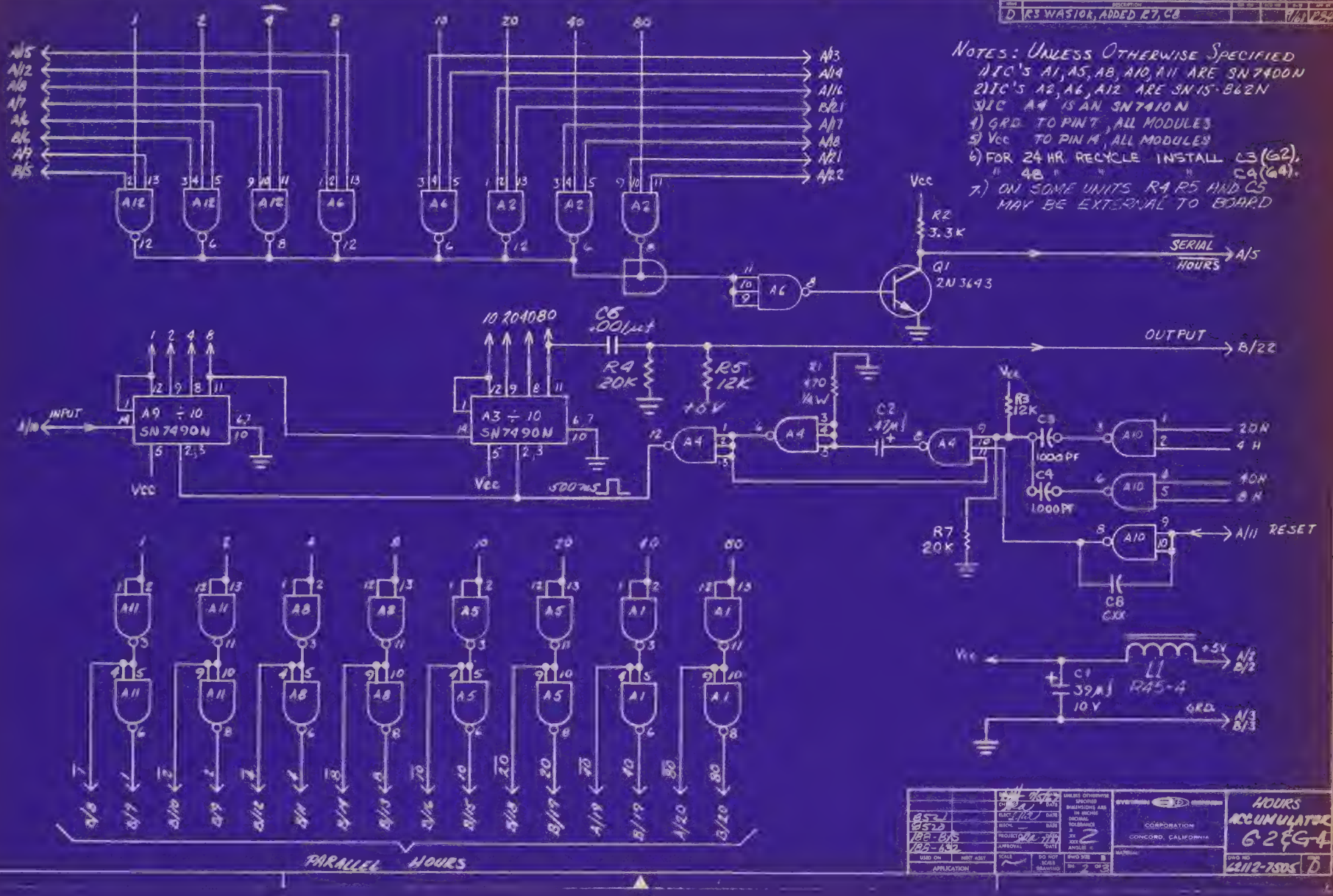
$\overline{\text{SERIAL HOURS}}$ is produced by sequentially gating each output line into transistor Q1. Each of the three input scan gates has two timing signals and one output line applied to it. The timing signals cause each output to be read at the proper time and therefore produces a serial output.

ACCUMULATORS (G1, G2, G3, G4) (Dwg. 62112-8505 G1, G2, G3, G4)

Ref.	Description	S-D Part No.
CAPACITORS		
C1	Capacitor, 39 µf, 10 V	C0902
C2	Capacitor, 0.47 µf, 35VV	C0733
C3	Capacitor, 1000 pf	C0543
C4	Capacitor, 1000 pf	C0543
C5	Capacitor, 0.001 µf, Disc	C0235
C6	Capacitor, 0.001 µf, Disc	C0235
C7	Capacitor, 470 pf, Mica	C0542
C8	Capcitor, CXXXX DM-15	
INTEGRATED CIRCUITS		
A1,55, 8, 10, 11	Integrated Circuit, SN7400N	19705
A4	Integrated Circuit, SN7410N	19706
A3, 9	Integrated Circuit, SN7490N	19711
A7	Integrated Circuit, SN7492N	23442
A2, 6, 12	Integrated Circuit, SN15-862N	19719
TRANSISTORS		
Q1	Transistor, 2N3643	Q0179
RESISTORS		
R1	Resistor, CC, 470 Ω, 1/4 W, 5%	R1044
R2	Resistor, CC, 3.3 kΩ, 1/4 W, 5%	R0742
R3, 5	Resistor, 12 kΩ , 1/4 W, 5%	R0759
R4	Resistor, CC, 20 kΩ, 1/4 W, 5%	R0964
R6	Resistor, CC, 330 Ω, 1/4 W, 5%	R0662

ACCUMULATOR (G1, G2, G3, G4)
P/L 62112-8505 G1, G2, G3, G4
CONTINUED

Ref.	Description	S-D Part No.
RESISTORS (continued)		
R7	Resistor, CC, 20 kΩ, 1/4 W, 5%	R0964
OTHER		
L1	Inductor, R45-4	L0143
	Schematic	B62112-7505
	Assembly	B62112-4505


D R3 WAS10K, ADDED R7, C8
NOTES: UNLESS OTHERWISE SPECIFIED
1) IC'S A1, A5, A8, A10, A11 ARE SN7400N
2) IC'S A2, A6, A12 ARE SN15-862N
3) IC A4 IS AN SN7410N
4) GRD TO PIN 7, ALL MODULES
5) Vcc TO PIN 14, ALL MODULES
6) FOR 24 HR. RECYCLE INSTALL C3 (G2), 48 " " " C9 (G4).
7) ON SOME UNITS R4 R5 AND C5 MAY BE EXTERNAL TO BOARD
A/5
A/12
A/6
A/7
A/4
A/8
A/9
B/5
A/3
A/14
A/16
B/21
A/17
A/18
A/21
A/22
A12
A6
A2
A4
A9 ÷ 10 SN7490N
A3 ÷ 10 SN7490N
A10
A11
A8
A5
A1
Vcc
R2 3.3K
Q1 2N3643
SERIAL HOURS
R4 20K
R5 12K
+10 V
C6 .001μf
R1 470 1/4W
C2 .47μf
R3 12K
C3 1000 PF
C4 1000 PF
R7 20K
C8 CXX
OUTPUT B/22
INPUT A/10
500 nS
20N 4 H
40N 8 H
A/11 RESET
C1 39μf 10 V
L1 R45-4
+5V A/2 B/2
GRD A/3 B/3
PARALLEL HOURS
HOURS ACCUMULATOR G2 & G4
DRG NO 62112-2505
REV D

6.7 CONTROL, INPUT/OUTPUT (Dwg. B62112-7508 G3)

GENERAL

This card performs three functions. It contains a circuit to process a signal from WWV to extract the 1 sec tick, a circuit to generate a DC serial output code, and a circuit to generate a modulated serial code.

WWV CIRCUIT

The audio signal from a WWV receiver is fed into a circuit which amplifies the 5 cycles of 1 kHz which comprise the 1 second "tick" and rejects everything else. The operation of Q8, Q9, and Q10 is identical to that of the sine wave shaper described below in the modulated code section. The output from this 1 kHz filter is further processed by the diode/RC network on the base of Q10. When sufficient amplitude has built up (about 2 cycles) Q10 conducts, producing a negative going pulse at pin B/22 and, via Q11, a positive going pulse at A/15.

DC CODE CIRCUIT

The DC code is produced by flip-flop A4. This flip-flop is set to the one state every 10 ms. Reset is controlled by an array of gates to provide three different pulse lengths. An 8 ms pulse is a MARK, 5 ms a ONE, and 2 ms a ZERO. The timing diagram, Figure 1, shows the relationship of the various signals used to control the reset time. Gate A1-11 provides a reset signal 8 ms after the flip-flop is triggered on; Gate A5-8 provides reset at 5 ms; AND gate A5-6 provides reset at 2 ms. The output of these three gates are paralleled, therefore reset will occur at the earliest reset provided.

The DC code is fed to the modulated code circuit and, through buffer A2-I2, to the DC code output connector.

MODULATED CODE CIRCUIT

The modulated code is produced by taking the I kHz square wave converting it to a sine wave and varying the amplitude with the DC code signal.

The I kHz square wave at pin A16 is inverted by gate A1-3, integrated by RI and C2 and applied to the base of constant current generator Q3. QI is an amplifier with C4 providing capacitive feedback. This makes the amplifier appear to have an inductive reactance. Capacitor C5 gives the circuit the electrical properties of a tuned circuit, with R4 providing fine frequency adjustment. R3 is factory selected to allow R4 to cover the desired adjustment range.

The modulator consists of a resistive network and a field effect transistor, used as a switch. Resistors RI2, RI3, and RI5, and potentiometer RI4 set the *"MARK TO SPACE RATIO"*. The F.E.T., Q4 switches from a virtual open circuit to a low impedance at a rate determined by the DC code signal on its gate. This causes the resistance ratio to change, changing the voltage which is fed to the output amplifier.

The output amplifier, A6, provides a low impedance source and allows adjusting (with R27) the peak output voltage.

PARTS LIST

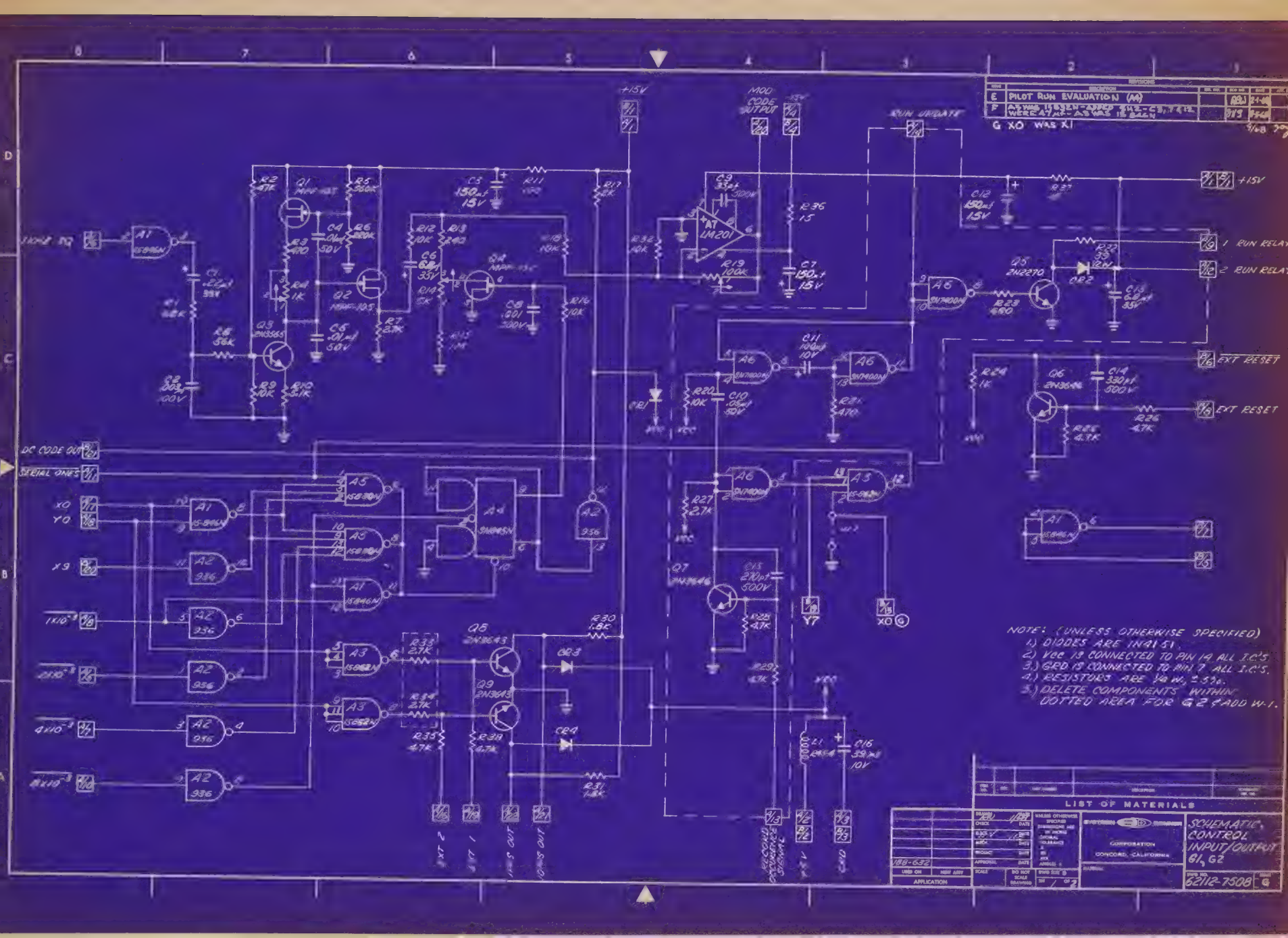
CONTROL, INPUT/OUTPUT P/L 62112-8508 (G1, G2, G3, and G4)

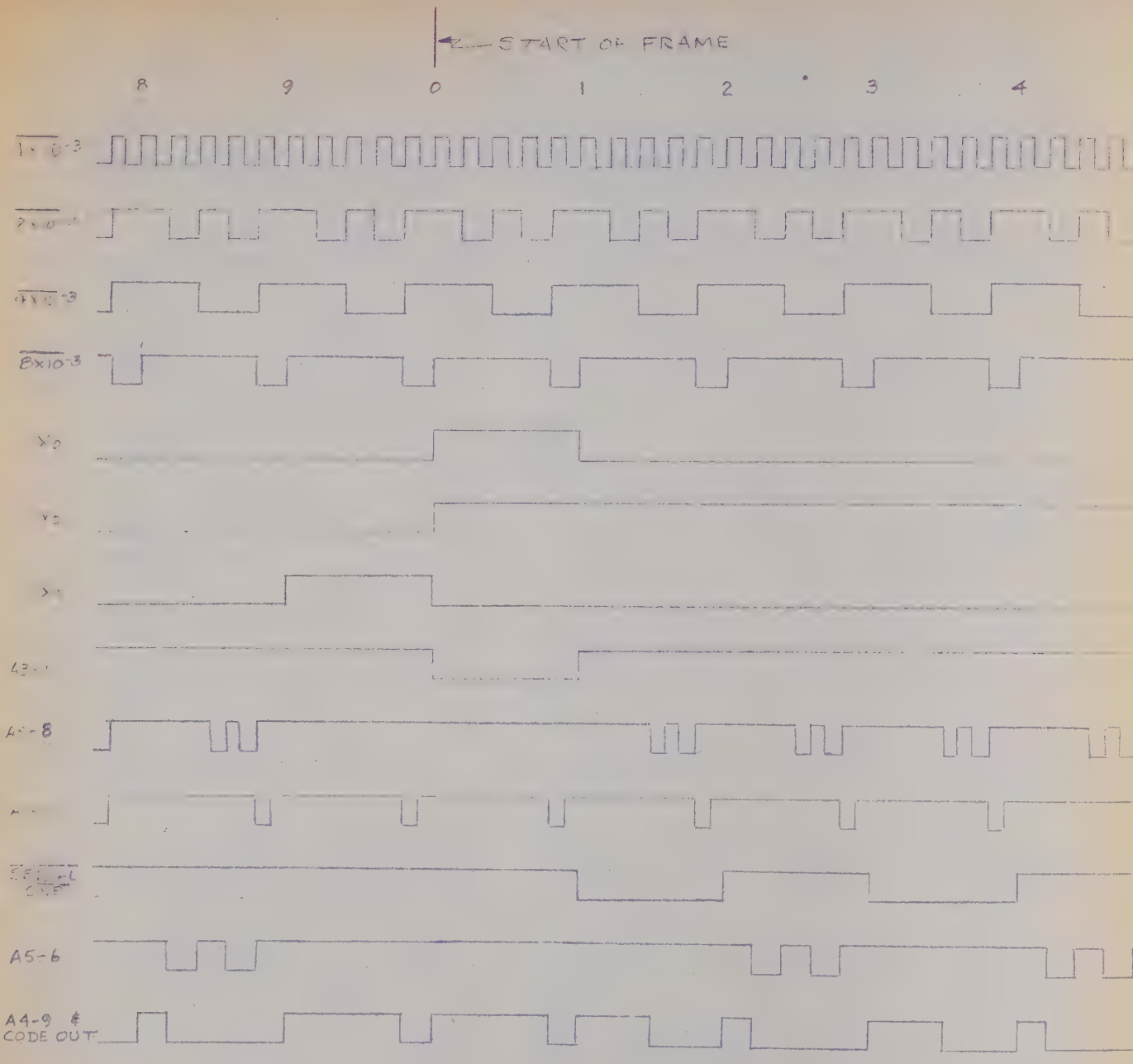
Ref.	Description	S-D Part No.
CAPACITORS		
	Capacitor, 0.22 µf, 35V	C0354
	Capacitor, 0.0033 µf, 300V	C0999
	Capacitor, 0.01 µf, 50V	C0705
	Capacitor, 0.47 µf, 35V	C0917
	Capacitor, 47 µf, 20V	C0924
	Capacitor, 0.001 µf, DM15	C0543
	Capacitor, 33 pf, DM15	C0531
	Capacitor, 6.8 µf, 35V	C0900
	Capacitor, 0.05 µf, 50V	C0708
	Capacitor, 100 µf, 10VV	C0660
	Capacitor, 330 pf, DM15	C0540
	Capacitor, 270 pf, 500V	C0539
	Capacitor, 39 µf, 10V	C0902
	Capacitor, Mylar, 0.22 µf, 200V	C1033
	Capacitor, Disc, 0.01 µf, +80-20%, 100V	C0556
	Capacitor, Disc, 0.03 µf, 50V	C0859
	Capacitor, Disc, 0.1 µf, 50V	C0881
	Capacitor, Tant, 150 µf, ±10%, 15V	C1026
	Capacitor, 100 pf, DM15	C0536
DIODES		
	Diode, IN4151	CR0150
	Diode, IN725A (Zener)	CR0064

CONTROL, INPUT/OUTPUT
P/L 62112-8508 (G1, G2, G3, and G4)
CONTINUED

Ref.	Description	S-D Part No.
INTEGRATED CIRCUITS		
	Integrated Circuits, SNI5-846N	I9716
	Integrated Circuits, MC-836P	25704
	Integrated Circuits, SNI5-845N	I9715
	Integrated Circuits, SNI5-830N	I9712
	Integrated Circuits, SN7400N	Q0237
	Integrated Circuits, SNI5-862N	I9719
	Integrated Circuits, LM-207	25700
TRANSISTORS		
	Transistor, 2N3565	Q0237
	Transistor, 2N3643	Q0179
	Transistor, 2N3646	Q0218
	Transistor, 2N2270	Q0102
	Transistor, MPF-105	Q0264
	Transistor, MPF-152	Q0263
RESISTORS		
	Resistor, CC, 68 kΩ, 1/4 W, 5%	R0891
	Resistor, CC, 55 kΩ, 1/4 W, 5%	R1235
	Resistor, CC, 10 kΩ, 1/4 W, 5%	R0766
	Resistor, CC, 5.1 kΩ, 1/4 W, 5%	R0693
	Resistor, CC, 47 kΩ, 1/4 W, 5%	R0777
	Resistor, CC, 470 Ω, 1/4 W, 5%	R1044
	Resistor, CC, 560 kΩ, 1/4 W, 5%	R1321
	Resistor, CC, 220 kΩ, 1/4 W, 5%	R0967

Ref.	Description	S-D Part No.
RESISTORS (continued)		
	Resistor, CC, 2.1 kΩ , 1/4 W, 5%	R0937
	Resistor, CC, 240 Ω, 1/4 W, 5%	R0835
	Resistor, CC, 1 MΩ, 1/4 W, 5%	R0962
	Resistor, CC, 100 Ω, 1/4 W, 5%	R0966
	Resistor, CC, 2 kΩ, 1/4 W, 5%	R0734
	Resistor, CC, 15 Ω, 1/4 W, 5%	R1607
	Resistor, CC, 4.7 kΩ, 1/4 W, 5%	R0892
	Resistor, CC, 1.8 kΩ, 1/4 W, 5%	R0959
	Resistor, CC, 1 kΩ, 1/4 W, 5%	R0765
	Resistor, CC, 39 Ω, 1/2 W, 5%	R0724
	Resistor, VARI., 1 kΩ, 1/4 W, 5%	R2248
	Resistor, VARI., 5 kΩ, 1/4 W, 5%	R2174
	Resistor, VARI., 100 kΩ, 1/4 W, 5%	R2191
	Resistor, CC, 680 Ω, 1/4 W, 5%	R1234
	Resistor, CC, 910 Ω, ±5%, 1/4 W	R1795
	Resistor, CC, 100 kΩ, ±5%, 1/4 W	R0741
	Resistor, CC, 15 kΩ, ±5%, 1/4 W	R0728
	Resistor, CC, 6.2 kΩ, ±5%, 1/4 W	R0965
	Resistor, CC, 2 kΩ, ±5%, 1/4 W	R0734
	Resistor, VARI, 1 kΩ	R1288
	Resistor, VARI, 5 kΩ	R2424
	Resistor, VARI, 100 kΩ	R2426
OTHER		
	Inductor, R45-4	L0143
	Schematic	62112-7508
	Assembly	62112-4508


E PILOT RUN EVALUATION (AA)
F AS WAS IS NOW - ADD R32-C9 WERE AT AF - AS WAS IS NOW
G XO WAS X1
+15V
MOD CODE OUTPUT
RUN UPDATE
1 RUN RELAY
2 RUN RELAY
EXT RESET
EXT RESET
DC CODE OUT
SERIAL ONES
XO
YO
X9
1X10^-3
2X10^-3
4X10^-3
8X10^-3
EXT 2
EXT 1
TENS OUT
ONES OUT
Y7
XO
NOTE: (UNLESS OTHERWISE SPECIFIED)
1.) DIODES ARE IN4151.
2.) Vcc IS CONNECTED TO PIN 14 ALL I.C.'S
3.) GRD IS CONNECTED TO PIN 7 ALL I.C.'S.
4.) RESISTORS ARE 1/4 W, 5%.
5.) DELETE COMPONENTS WITHIN DOTTED AREA FOR G2 & ADD W-1.
LIST OF MATERIALS
SCHEMATIC, CONTROL INPUT/OUTPUT G1, G2
52112-7506
G

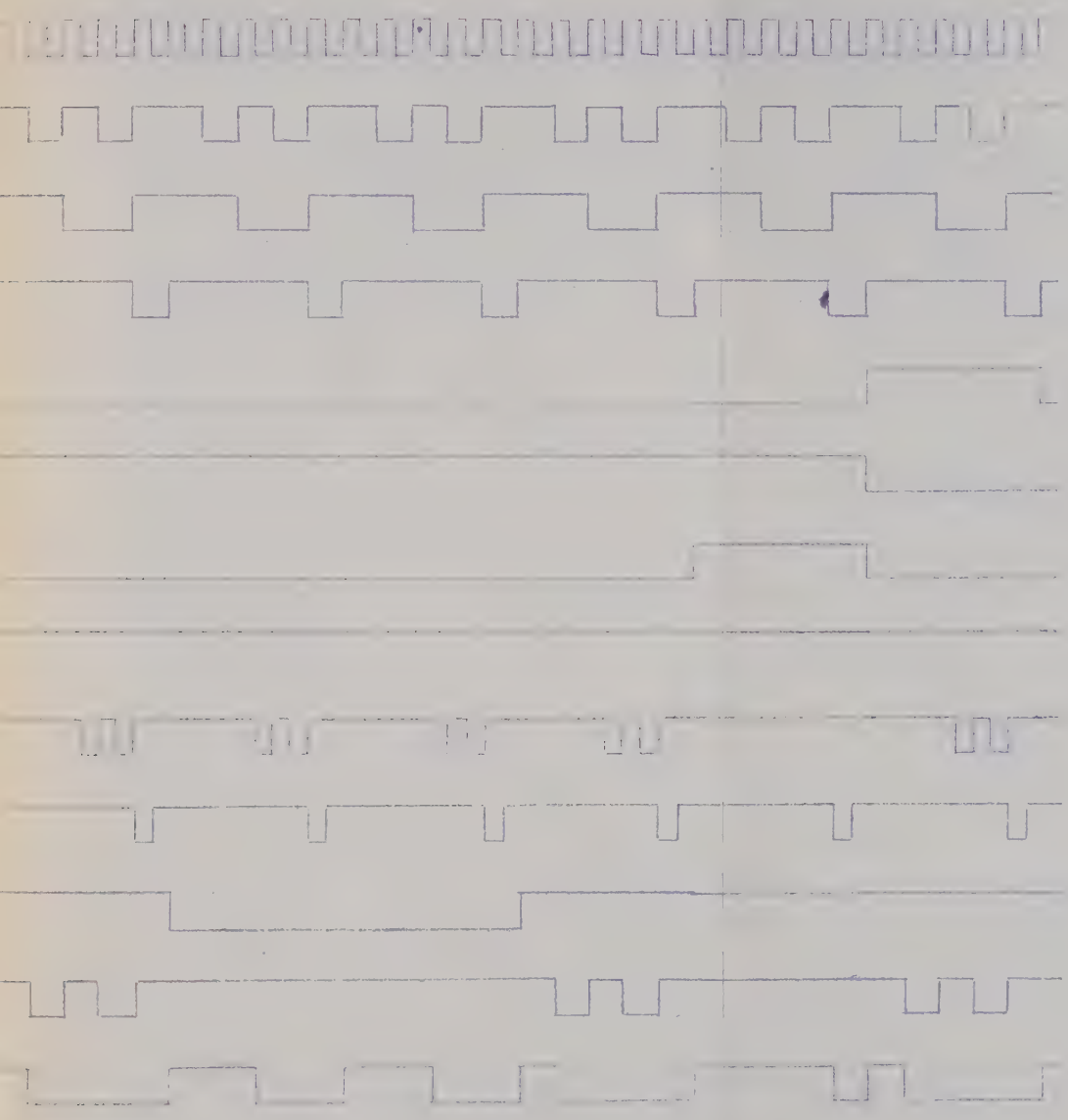

START OF FRAME
8
9
0
1
2
3
4
1x10-3
2x10-3
4x10-3
8x10-3
X0
Y0
X1
A3-1
A1-8
A7-1
A5-6
A4-9 & CODE OUT

2 1

REVISIONS

ISSUE	DESCRIPTION	SER NO	ECO NO	DATE	APP BY

6 7 8 9 0 1



10 MS

6-38

		DRAWN DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCES X .X .XX ANGLE	BYSTRON DONNER CORPORATION CONCORD CALIFORNIA	TIMING DIAGRAM IRIG [illegible]
		CHECK DATE			
		ENGR DATE			
		PROJECT DATE			
352		APPROVAL DATE			
USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING	DWG SIZE B	DWG NO G 3 ISSUE
APPLICATION				MATERIAL	

6.8 POWER SUPPLY (Dwg. B62211-7306, A62211-7307, A62211-7114, B62211-7305)

GENERAL

The power supply provides four voltage from a switching regulator controlled dc to dc converter. The voltage are +15, -15, +5, and +200 V dc. The input to the supply is from one of three sources: A built-in (Optional) ac power supply, an external dc voltage (28 V nominal, 12 to 50 V dc) or a built-in (Optional) rechargeable battery pack. Provision is made for automatic, instantaneous changeover to the internal batteries should external power fail.

INPUT AND CONTROL CIRCUIT (Refer to Dwg. B62211-7306)

The external dc power source enters the unit through a PI section filter network (A62211-4110). Diodes CR5 and CR15 allow operating the optional battery heater and the display control relay at all times when dc power is applied or when the ac supply is on. Diodes CR6 and CR7 form a switch to automatically connect the batteries whenever the input voltage is below the battery voltage. Resistor R4 and diode CR8 permit battery charging when the unit is turned on. Relay K1 controls the 200 V for the illuminated display when the unit is operating. Its primary function is to disconnect the display from the power supply during battery operation to conserve power. The "BATTERY DISPLAY" switch permits turning on the display, momentarily. When the unit is operating from either the ac supply or an external dc voltage, K1 will be held on by diode CR15, keeping the display on. Resistor R6 is used to prevent K1 from energizing when the battery voltage drops below 12 V. In this way, the "BATTERY DISPLAY" switch serves as

a "near-end-of-operation" test for the battery; i.e. when the display does not light with the switch depressed, the battery is nearing its minimum voltage point. The ac supply is diode coupled to the input circuit and automatically powers the unit when turned on.

AC POWER SUPPLY - OPTIONAL (Dwg. B62211-7114)

The ac power supply accepts 115/230 V (selected internally with a switch), through a line filter, and delivers 28 V dc through two diode isolated outputs. Diodes CR1 and CR2 form a full wave rectifier , diodes CR3 and CR4 are used to isolate the supply from the other voltage sources in the unit.

SWITCHING REGULATOR

The switching regulator accepts an input of 12 to 50 V dc and supplies a regulated voltage of approximately 12 V to the dc to dc converter. Refer to Dwg. 62211-7307. Transistor Q5, zener diode CR4, and potentiometer R14 form an adjustable current source. The current generated flows through R12, producing a constant voltage across the resistor. In this way the voltage at Q4 base follows the regulated voltage and the offset is adjustable. The voltage is applied to the Schmitt Trigger (Q2 and Q3) through emitter follower Q4 and zener diode CR3. The Schmitt Trigger causes Q1 to conduct when the voltage drops below the set point. This cause Q1 (on Dwg. B62211-7306) to conduct, producing a pulse of voltage. The voltage pulse is applied to capacitors C3, C4, and C7 (Dwg. B62211-7307) through inductor L1 (Dwg. B62211-7306). When the voltage reaches the set point, the Schmitt Trigger turns off, terminating the voltage pulse. A series of pulses is produced to keep the voltage on the capacitors at the set point. The network composed of L1, C3, C4, and C7

smoothes the pulses to give a steady voltage. Zener diode CR13 is used to shut off the regulator when the input voltage is less than 12 V.

DC TO DC CONVERTER

The voltage from the switching regulator is applied to the center point of the collector winding of T1 (Dwg. B622II-7306). Bias for the base winding center point is provided by R7 and R17 (on Dwg. A622II-7307). Q2 and Q3 (Dwg. B622II-7306) along with R1 form a free-running oscillator which produces square wave ac on the three output windings. One winding supplies +5 V through a full wave rectifier, CR11, CR12 (Dwg. B622II-7306); another 200 V through a full wave bridge rectifier CR9-12 (Dwg. A622II-7307); and the third +15 V and -15 V through full wave rectifiers CR5, CR8, and CR6, CR7.

BATTERY HEATER - OPTIONAL (Dwg. B622II-7305)

The battery heater allows operation down to -55°C. Thermistor RT1 senses the battery temperature by changing its resistance with changes in temperature. Zener diode CR1 provides a regulated voltage for the input voltage divider and the Schmitt Trigger. The voltage change at Q1 base is coupled by Q1 (as an emitter follower) into the Schmitt Trigger Q2, Q3. A decrease in temperature causes RT1 to increase resistance, thereby increasing the voltage at Q1 emitter. This causes Q3 to turn on, turning on Q4, Q5, and thus, the heater.

PARTS LIST

BATTERY PACK P/L 62211-8301 (G1 and G2)

Ref.	Description	S-D Part No.
BT1, 2	Battery (Gulton 8 V 0.750)	BT0002
RT1	Thermistor, GE 1D01	
J9	Conn. Winch MRE5-3SN7HVL	J0573
	Schematic	B62211-7305
	Assembly	C62211-4301

PARTS LIST

TRANSFORMER BRACKET ASSEMBLY P/L 21790-8

Ref.	Description	S-D Part No.
CAPACITORS		
C5	Capacitor, 0.01 µf	C0341
DIODES		
CR10	Diode, IN4002	CR0276
CR11, 12	Diode, IN1201A	CR0295
CR9	Diode, IN4005	CR0284
RESISTORS		
R8	Resistor, 250 Ω, 5 W	R2360
R7	Resistor, 56 Ω, 1/4 W	R1554
TRANSISTORS		
Q1-3	Transistor, 2N3715	Q0223
OTHER		
T1	Transformer	C21791
L1	Inductor, 4 mh, TT2320	2119-10182
K1	Relay, Babcock BR8-600-B3-26 V	
	#6-32 Float Pem	H0811
	Standoff	E0098
	Standoff	E0131
	Schematic	B62211-7306
	Assembly	B21790-4

PARTS LIST

COMPONENT BKT. DC POWER SUPPLY P/L 62211-8112 (G1, G2, G3)

Ref.	Description	S-D Part No.
CAPACITORS		
C3	Capacitor, 1100 µf, 50 B, (39 D)	C1103
C4	Capacitor, 0.33 µf, 400 V	C1131
DIODES		
CR6, 7	Diode, IN1201A	CR0295
CR5, 8, 14, 15	Diode, IN4005	CR0284
RESISTORS		
R3	Resistor, 220 k, 1/2 w	R0264
R4	Resistor, 100 Ω, 5 w	R1674
R5	Resistor, 560 Ω, 1 w	R1668
R6	Resistor, 220 Ω, 1/4 w	R0760
OTHER		
	Schematic	B62211-7306
	Assembly	A62211-4112

PARTS LIST

LINE FILTER ASSEMBLY P/L 62211-8110

Ref.	Description	S-D Part No.
	Capacitor, 0.1 µf, ±20%, 50 V	C0781
	Inductor, Miller 5248, 68 µh, 2A	L0151

PARTS LIST

AC POWER SUPPLY P/L 62211-8114

Ref.	Description	S-D Part No.
CAPACITOR		
C1	Capacitor, 1100 µf, 50 v, Spr39D	C1103
DIODES		
CR1, 2, 4	Diode, IN1201A	CR0295
CR3	Diode, IN4002	CR0276
OTHER		
	Terminal	E0098
Z1	Line Filter, GFI162	L0038
F2	Fuse, 1/2 H, 3AG, S10 B10	F0012
XF2	Fuse Holder	X0034
P10	Connector, Amph 264100-8P	J0557
	Schematic	62211-7114
	Assembly	62211-4114

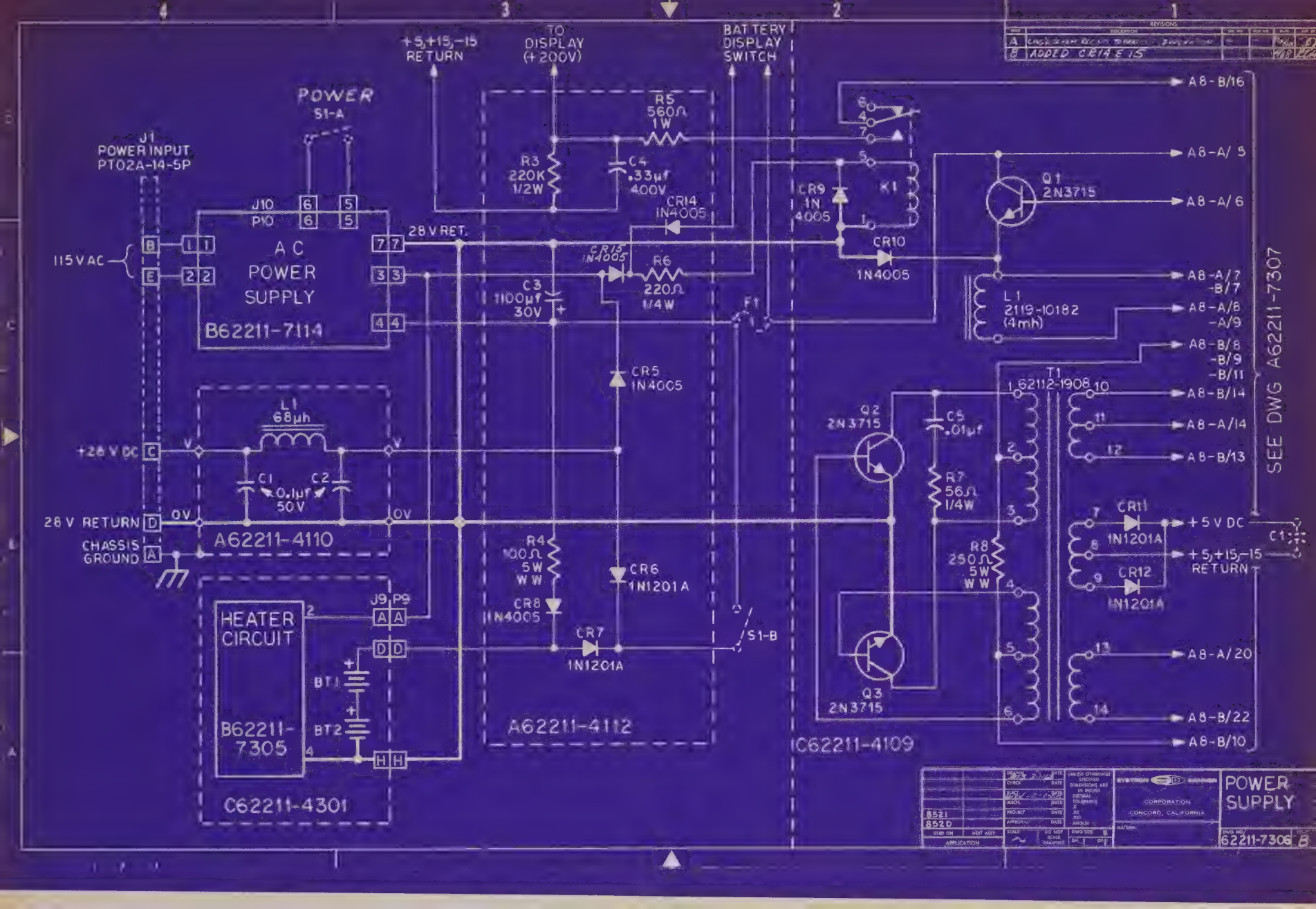
PARTS LIST

SWITCHING REGULATOR P/L 62112-8509

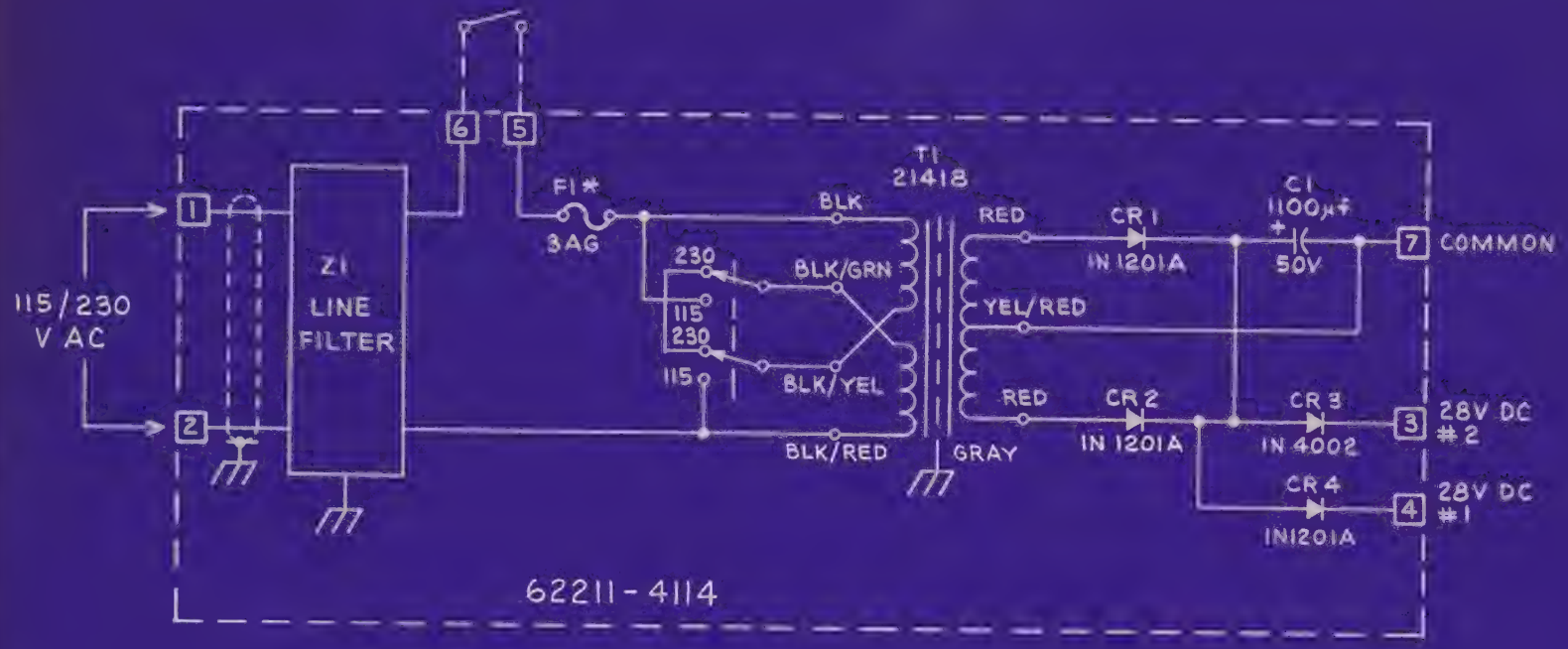
Ref.	Description	S-D Part No.
CAPACITORS		
C1	Capacitor, 1 µf, 20 V	C0524
C2	Capacitor, 150 pf,	C0537
C3, 4, 7	Capacitor, 150 µf, 15 V	C1026
C5	Capacitor, 0.1 µf, 200 V	C0987
C6, 8	Capacitor, 0.01, Ceramic Disc	C0341
C9, 10	Capacitor, 47 µf, 35 V	C0982
C11	Capacitor, 0.33 µf, 400 V, Electron, D4-334	C1131
DIODES		
CR1	Diode, 1N4739	CR0340
CR2	Diode, 1N4002	CR0276
CR3, 4	Diode, 1N702	CR0126
CR5-12	Diode, 1N4005	CR0284
CR13	Diode, 1N756A	CR0346
TRANSISTORS		
R1	Resistor, 470 Ω, 2 W, 5%, CC	R2082
R2	Resistor, 4.7 kΩ, 1/4 W, 5%, CC	C0892
R3	Resistor, 470 Ω, 1/4 W, 5%, CC	R1044
R4	Resistor, 30 Ω, 1/4 W, 5%, CC	R1549
R5	Resistor, 1 kΩ, 1/4 W, 5%, CC	R0765
R6, 7	Resistor, 1.8 kΩ, 1/4 W, 5%, CC	R0959
R8	Resistor, 1.2 kΩ, 1/4 W, 5%, CC	R0809
R9, 11	Resistor, 2.2 kΩ, 1/4 W, 5%, CC	R0749

SWITCHING REGULATOR
P/L 62112-8509
CONTINUED

Ref.	Description	S-D Part No.
RESISTORS (continued)		
R10	Resistor, 150 Ω, 1/4 W, 5%, CC	R0983
R12, 15	Resistor, 5.6 kΩ, 1/4 W, 5%, CC	R0821
R14	Resistor, 5 kΩ, Variable WW (Bourns)	R2335
R16	Resistor, 56 Ω, 1/4 W, 5%, CC	R1554
R17	Resistor, 30 Ω, 2 W, 5%, CC	R2267
R18	Resistor, 220 kΩ, 1/4 W, 5%, CC	R0264
R13	Resistor, 1.5 kΩ, 1/4 W, 5%, CC	R0783
TRANSISTORS		
Q1	Transistor, 2N2905	Q0259
Q2-5	Transistor, 2N2222	Q0116
OTHER		
	Schematic	62112-7509
	Schematic	62211-7307
	Assembly	62112-4509


REVISIONS
A
B ADDED CR14 & 15
+5,+15,-15 RETURN
TO DISPLAY (+200V)
BATTERY DISPLAY SWITCH
POWER
S1-A
J1
POWER INPUT
PT02A-14-5P
J10
P10
115 VAC
A C POWER SUPPLY
B62211-7114
28 V RET.
R5 560Ω 1W
R3 220K 1/2W
C4 .33μf 400V
CR14 IN4005
CR13 IN4005
R6 220Ω 1/4W
C3 1100μf 30V
F1
CR5 IN4005
CR9 1N 4005
K1
CR10 1N4005
Q1 2N3715
L1 2119-10182 (4mh)
A8-B/16
A8-A/5
A8-A/6
A8-A/7 -B/7
A8-A/8 -A/9
A8-B/8 -B/9 -B/11
SEE DWG A62211-7307
T1 62112-1908
A8-B/14
A8-A/14
A8-B/13
L1 68μh
+28 V DC
C1 .01μf 50V
C2
28 V RETURN
CHASSIS GROUND
A62211-4110
Q2 2N3715
C5 .01μf
R7 56Ω 1/4W
R8 250Ω 5W WW
CR11 1N1201A
CR12 1N1201A
+5 V DC
+5,+15,-15 RETURN
C1
R4 100Ω 5W WW
CR8 IN4005
CR6 1N1201A
CR7 1N1201A
S1-B
Q3 2N3715
A8-A/20
A8-B/22
A8-B/10
C62211-4109
HEATER CIRCUIT
B62211-7305
J9 P9
BT1
BT2
C62211-4301
A62211-4112
8521
8520
POWER SUPPLY
DWG NO. 62211-7306 B

REVISIONS					
LTR	DESCRIPTION	PER ECN	BY	CHK	APP'D
B	WAS 115V ONLY				9/63

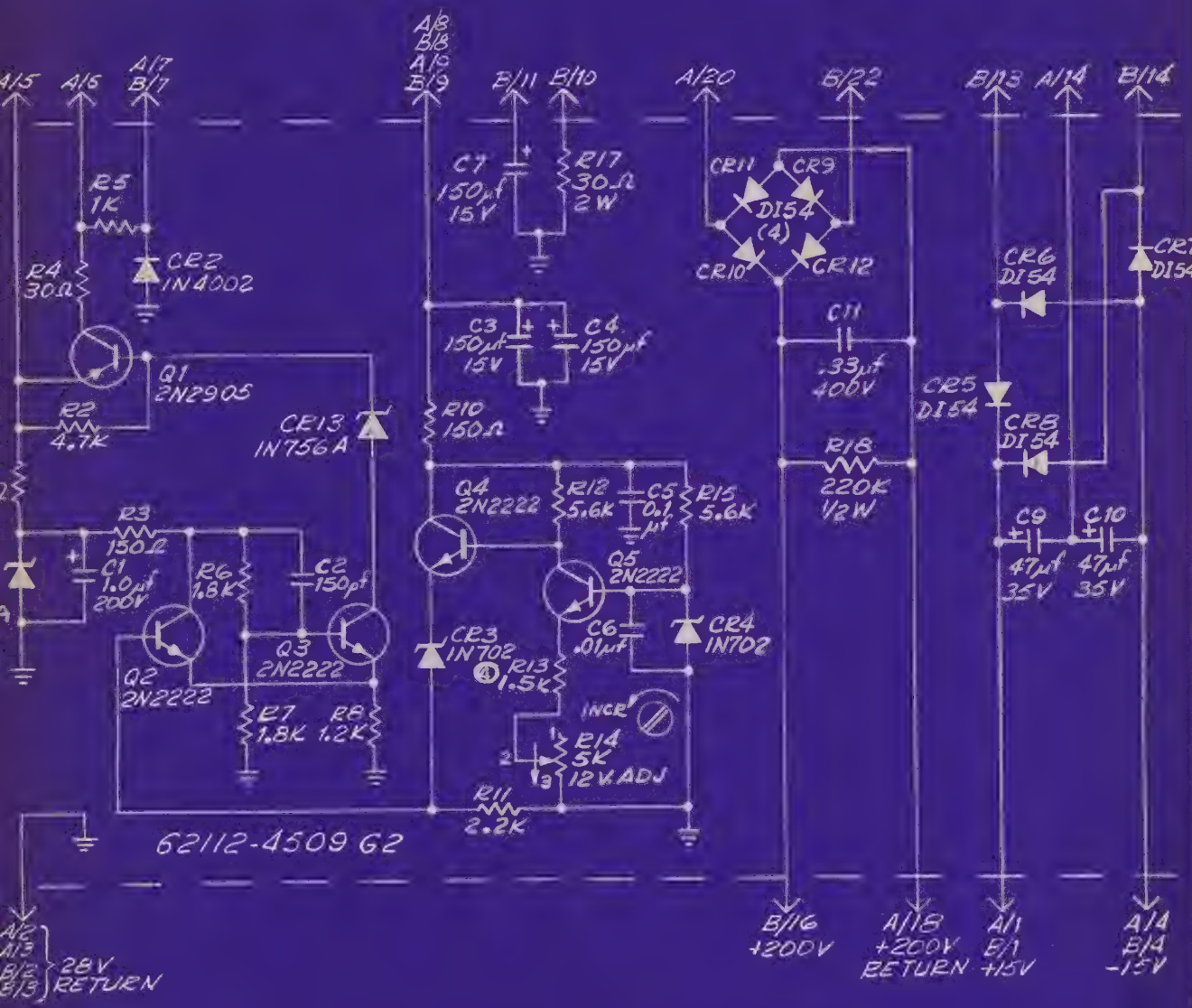


[nº] = PINS OF J10, "AMPHENOL #26-4200-8P, & THE MATE P10, "#26-4200-8S"

F1 = 1/2 A FOR 115V OPERATION.
1/4 A FOR 230V OPERATION.

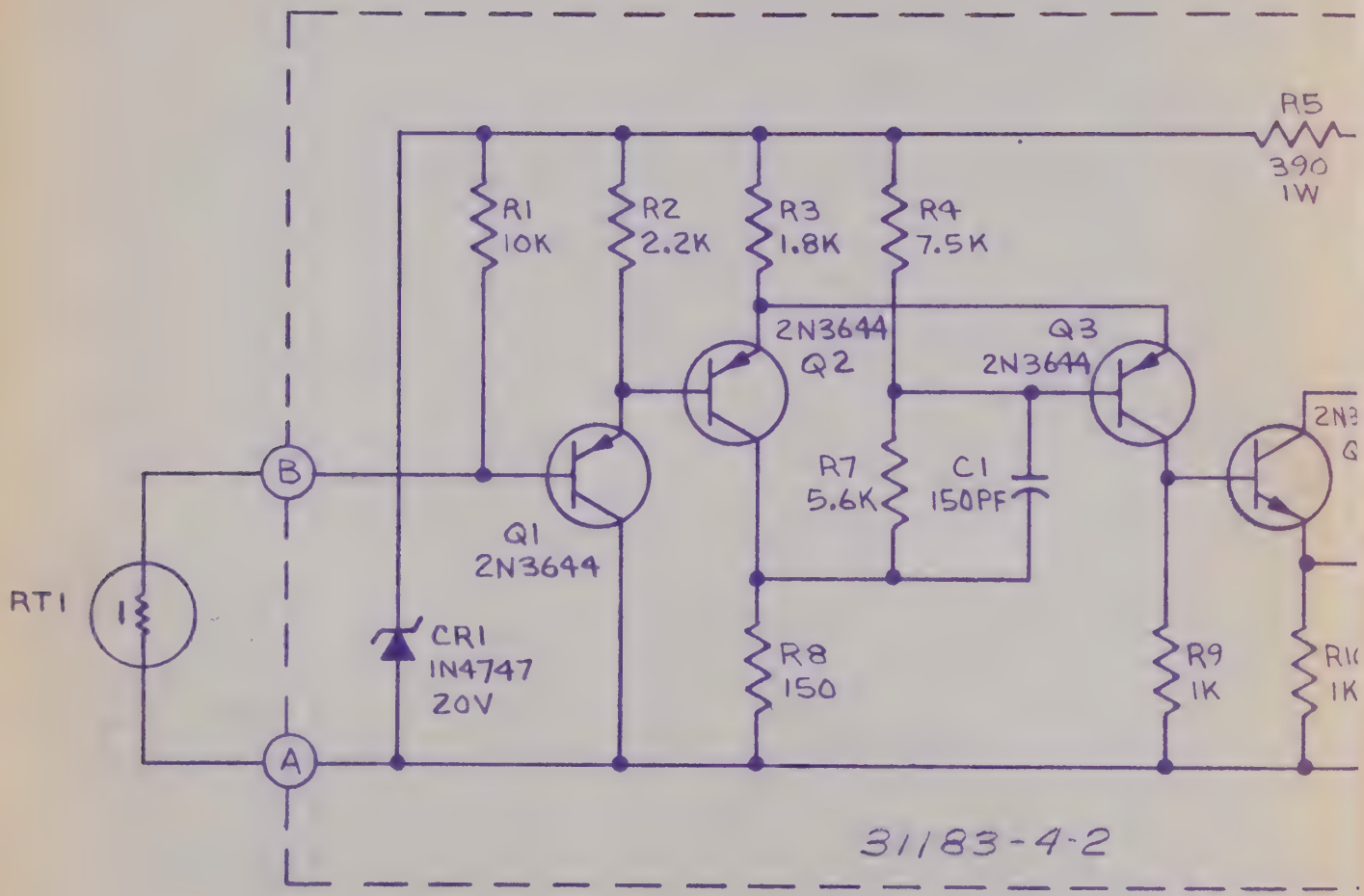
					AC POWER SUPPLY
8520 8521					DWG NO 62211-7114 B

REVISIONS				
DESCRIPTION	SER. NO.	ECO NO.	DATE	APP. BY:
R13 Was 2.2K			7/31/69	



NOTES
1. ALL RESISTORS ARE COMP. CARB. ±5% 1/4W

		DRAWN [illegible] DATE 2-1-68	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	SWITCHING REGULATOR	
		CHECK DATE				
		ELECT. DATE				
		MECH. DATE				
		PROJECT DATE				
		APPROVAL DATE				
D ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING	DWG SIZE B SH OF	MATERIAL P/N 62112-8509 G2	DWG NO. 62211-7307 ISSUE A
APPLICATION						

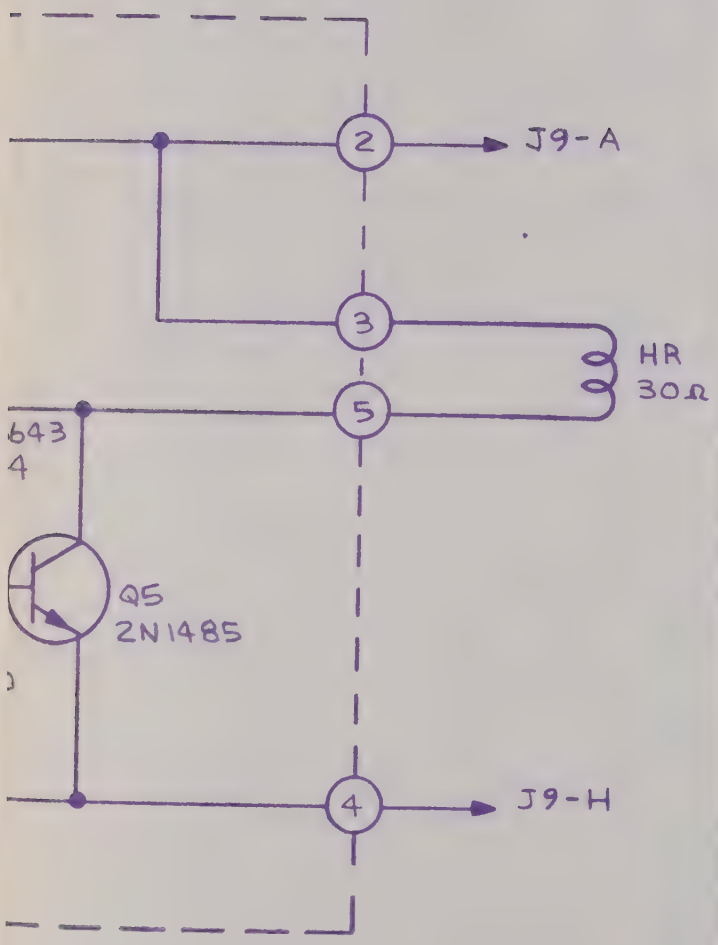


NOTE: (U

1. RESIST

REVISIONS

STAT	DESCRIPTION	SER NO	F NO	CTS	APP BY



NLESS OTHERWISE SPECIFIED)
ORS ARE IN OHMS, 1/4W, 5%.

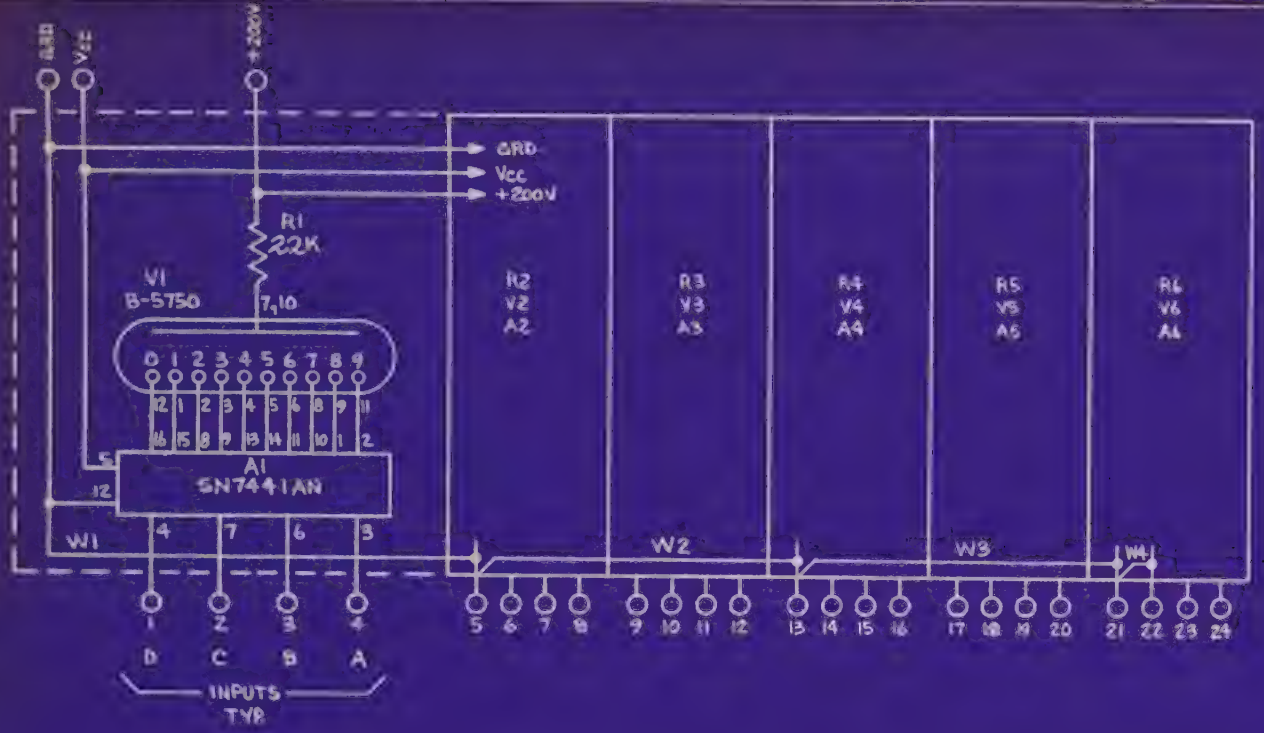
RBW 2-5-68

8521
8520

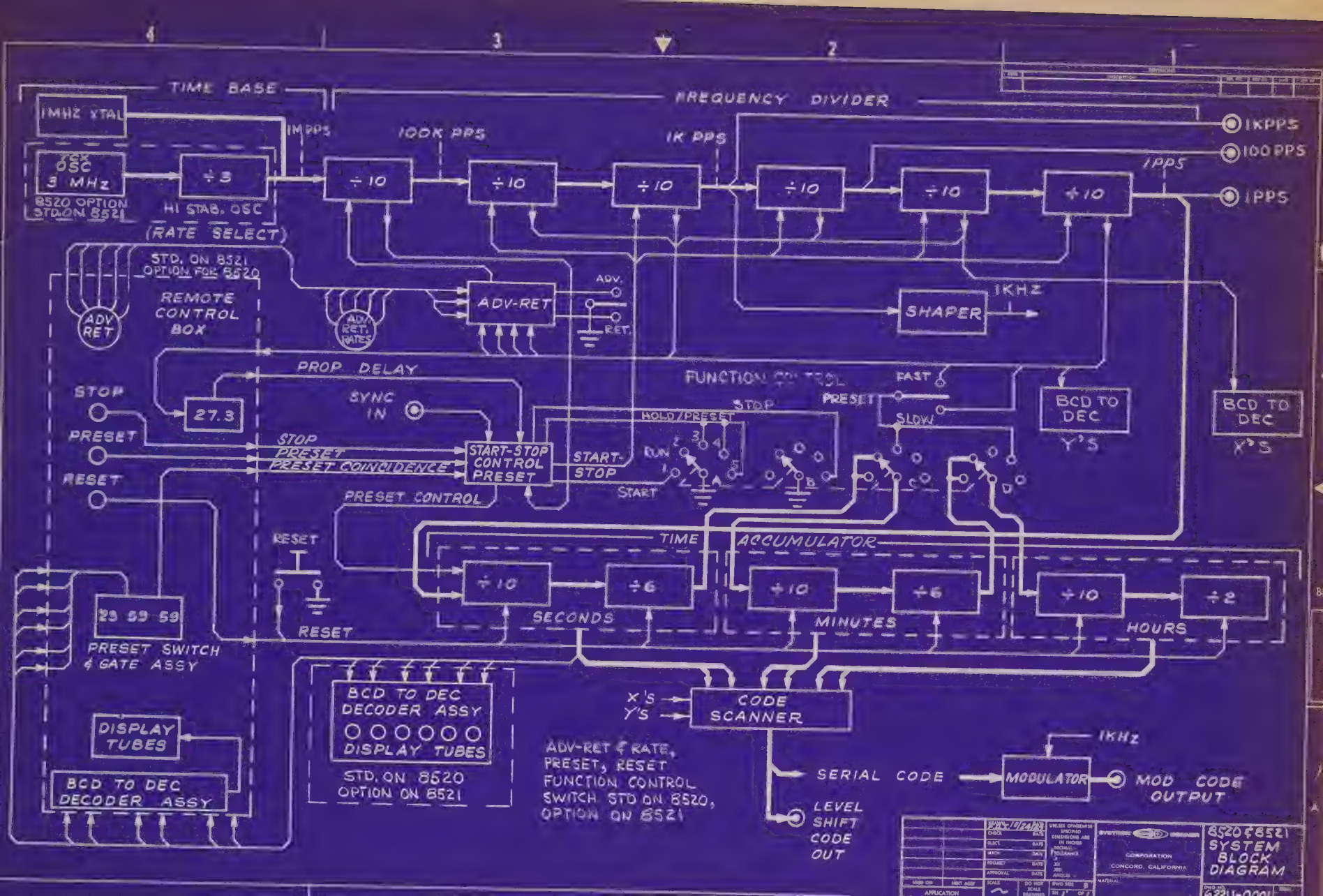
BYSTRON DONNER
CORPORATION
CONCORD, CALIFORNIA

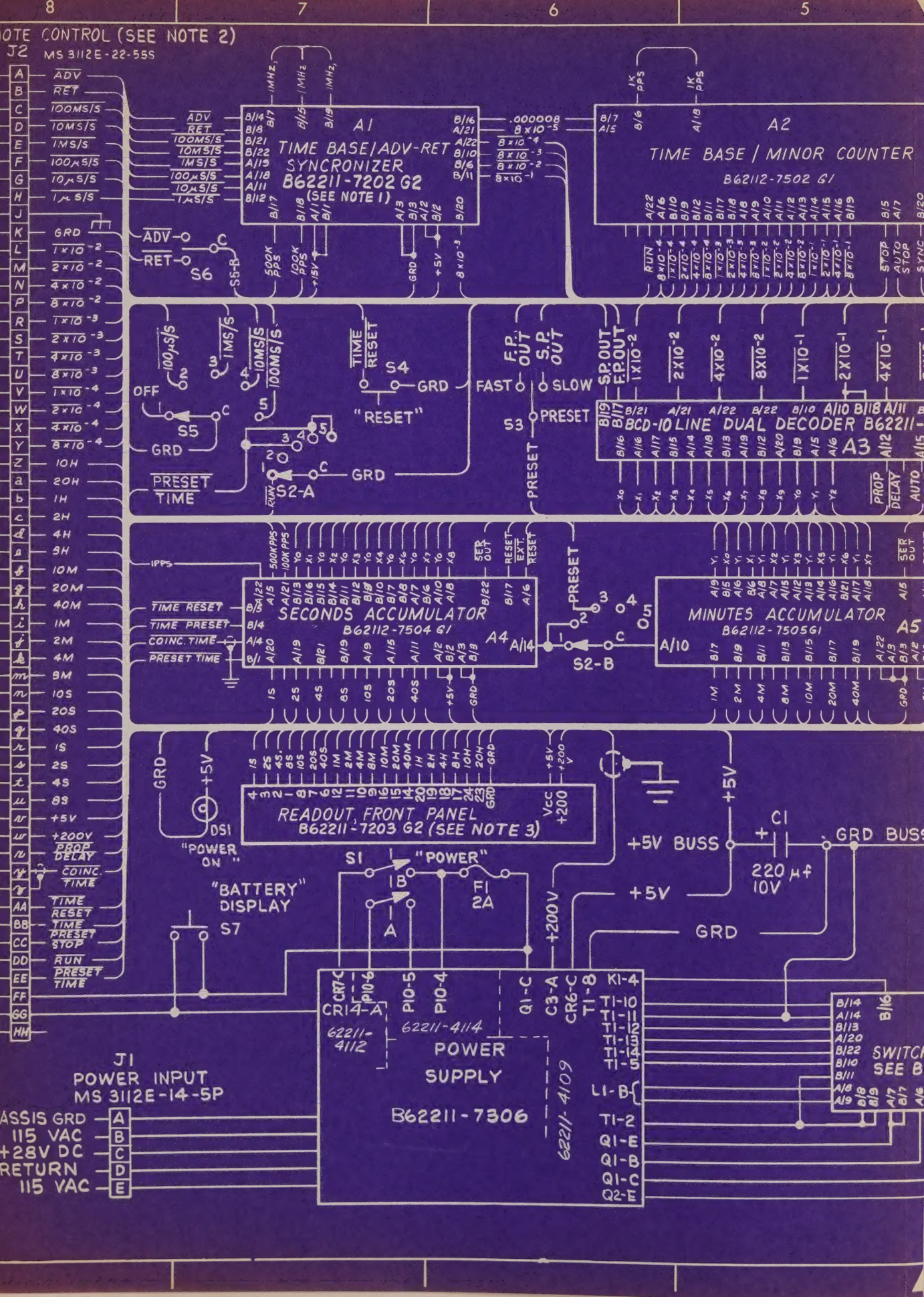
SCHEMATIC
HEATER
CIRCUIT

3/183-7-2 A

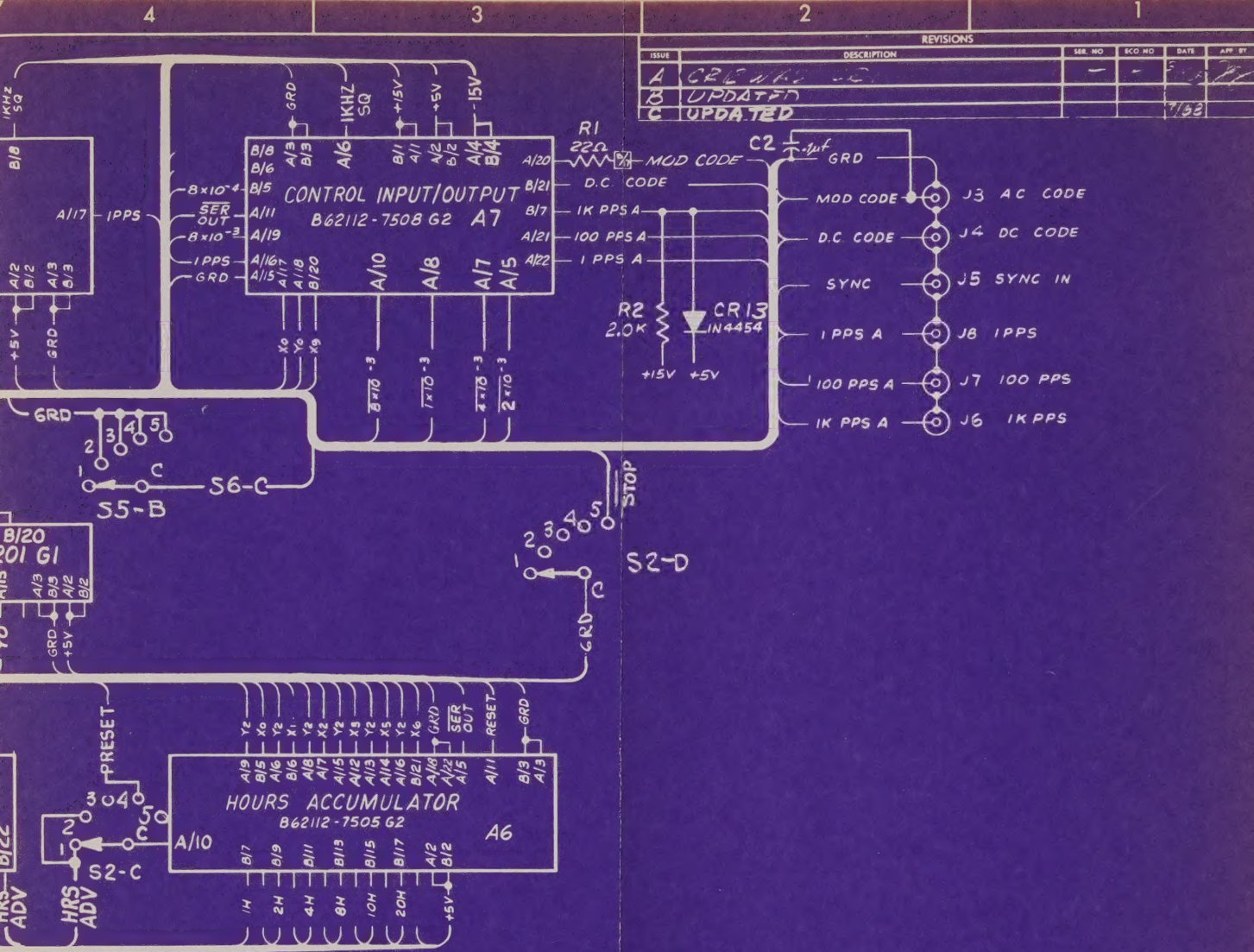


NOTE:
1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. CIRCUIT SHOWN IS TYPICAL (6) PLACES.
3. W1 - W4 ARE ON G2 ONLY.


TIME BASE
FREQUENCY DIVIDER
1MHZ XTAL
OCXO 3 MHz
8520 OPTION STD ON 8521
÷5
HI STAB. OSC
(RATE SELECT)
1MPPS
100K PPS
1K PPS
1PPS
1KPPS
100 PPS
1 PPS
÷10
÷10
÷10
÷10
÷10
÷10
STD. ON 8521 OPTION FOR 8520
REMOTE CONTROL BOX
ADV RET
ADV RET RATES
ADV-RET
ADV.
RET.
SHAPER
1KHZ
PROP DELAY
27.3
STOP
PRESET
RESET
SYNC IN
STOP
PRESET
PRESET COINCIDENCE
START-STOP CONTROL PRESET
START-STOP
START
HOLD/PRESET
STOP
RUN
PRESET
FAST
SLOW
BCD TO DEC Y'S
BCD TO DEC X'S
PRESET CONTROL
RESET
RESET
TIME ACCUMULATOR
÷10
÷6
÷10
÷6
÷10
÷2
SECONDS
MINUTES
HOURS
23 59 59
PRESET SWITCH & GATE ASSY
DISPLAY TUBES
BCD TO DEC DECODER ASSY
BCD TO DEC DECODER ASSY
DISPLAY TUBES
STD. ON 8520 OPTION ON 8521
X'S
Y'S
CODE SCANNER
ADV-RET & RATE, PRESET, RESET FUNCTION CONTROL SWITCH STD ON 8520, OPTION ON 8521
SERIAL CODE
1KHZ
MODULATOR
MOD CODE OUTPUT
LEVEL SHIFT CODE OUT
8520 & 8521 SYSTEM BLOCK DIAGRAM


8
7
6
5
NOTE CONTROL (SEE NOTE 2)
J2 MS 3112E-22-55S
A1
TIME BASE/ADV-RET SYNCRONIZER
B62211-7202 G2
(SEE NOTE 1)
A2
TIME BASE / MINOR COUNTER
B62112-7502 G1
A3
BCD-10 LINE DUAL DECODER B62211-
A4
SECONDS ACCUMULATOR
B62112-7504 G1
A5
MINUTES ACCUMULATOR
B62112-7505G1
READOUT, FRONT PANEL
B62211-7203 G2 (SEE NOTE 3)
POWER SUPPLY
B62211-7306
J1
POWER INPUT
MS 3112E-14-5P
CHASSIS GRD
115 VAC
+28V DC RETURN
115 VAC
"POWER ON"
"BATTERY" DISPLAY
"POWER"
"RESET"
+5V BUSS
GRD BUSS
220 µf 10V
+200V
S1
S2-A
S2-B
S3
S4
S5
S6
S7
DS1
F1 2A
1B
A
CR1
CR4-A
CR6-C
Q1-C
C3-A
T1-8
P10-6
P10-5
P10-4
62211-4112
62211-4114
62211-4109
SWITCH SEE B

REVISIONS					
ISSUE	DESCRIPTION	SER. NO	ECO NO	DATE	APP. BY
A	CREATED	—	—	5	
B	UPDATED				
C	UPDATED			7/22	



MODE CONTROL

S2	
POS. 1	START
2	RUN
3	MIN
4	HR.
5	STOP

NOTES:

1. 8521 USES B62211-7202 G1 ALSO 8520 WITH OPTION -5.
2. REMOTE CONTROL CONNECTOR DELETED ON 8520, UNLESS OPTION -3 OR -4 IS SELECTED.
3. READOUT DELETED ON 8521, UNLESS OPTION -3 IS SELECTED AND DELETED ON 8520 WITH OPTION -3.
4. SWITCHES S2-S7 DELETED ON 8521 AND ON 8520 WITH OPTION -3.

DRAWN JDL 2/29/68 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	MAIN CHASSIS WIRING DIAGRAM 8520-8521
CHECK DATE	DECIMAL TOLERANCE .X ±.1 .XX ±.01 .XXX ±.005 ANGLES ±		
ELEC. ENG 7/20/67 DATE		MATERIAL	DWG NO. 62211-7001 ISSUE C
MECH. DATE			
PROJECT DATE			
APPROVAL DATE			
USED ON / NEXT ASSY APPLICATION	SCALE ~ DO NOT SCALE DRAWING	DWG SIZE D SH 1 OF 1	

WARRANTY

Systron-Donner instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. This warranty does not apply to vacuum tubes, except as they are warranted by tube manufacturers. The liability of Seller under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer at his expense during such period and which has not been subjected to misuse, neglect, improper installations, repair, alteration, or accident. Seller shall have the right of final determination as to the existence and cause of a defect. In no event shall Seller be liable for collateral or consequential damages. This warranty is in lieu of any other warranty, express, implied or statutory, and no agreement extending or modifying it will be binding upon Seller unless in writing and signed by a duly authorized officer.

RECEIVING INSPECTION

Every Systron Donner instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the unit is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company.

REPAIRS

Whenever a Systron-Donner instrument requires service, the nearest Systron-Donner representative should be contacted; all representatives will provide immediate service or arrange factory returns when necessary.

Please specify both model and serial number in all correspondence concerning Systron-Donner instruments. Address all inquiries on operation or applications to your nearest sales representative or Sales Manager, Instruments, Systron-Donner Corporation, 888 Galindo Street, Concord, California.

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